EE273 Lecture 1
Introduction to Digital Systems Engineering

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Logistics

- See the course policy sheet for details

Lectures:	MW 11:00 to 12:15 in Skilling 193
Textbook:	Dally and Poulton, *Digital Systems Engineering*
Grading	25% 6 weekly problem sets 15% class project 25% midterm exam (10/26) 35% final exam
Collaboration	encouraged on problem sets and project groups of up to 3 people single solution all assistance acknowledged

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More Logistics

Course Staff	Professor	Bill Dally
	TAs	Kaushik Mittra Jin Namkoong
	Support	Shelley Russell
Late Policy	problem sets due at the ***beginning*** of class one week from the date of assignment ***no*** credit for late assignments	
	local SITN assignments and exams due at the same time	
	remote SITN assignments and exams due one week after this time	

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Yet More Logistics

Exams	Midterm	October 26 7PM-9PM No class that day Local SITN students must come to campus
	Final	December 10 8:30AM-10:30AM
Assignments	assigned each Wednesday due at ***beginning*** of class the following Wednesday	
Reading	assigned for each class. Complete reading ***before*** the corresponding class	

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Today's Assignment

- Reading
  - Chapter 1
  - Sections 3.1 through 3.3.3
  - Complete before next Monday 9/28
- Problem Set 1
  - Complete problems 1-1, 1-5, and 1-9 in the text
  - Due at the start of class on Wednesday 9/30

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What is Digital Systems Engineering

- System level electrical design
  - noise management
    - keeping signals clean
  - signaling
    - moving bits from here to there
  - timing
    - how we know when a new bit is here
  - power distribution
    - DC voltage with AC current

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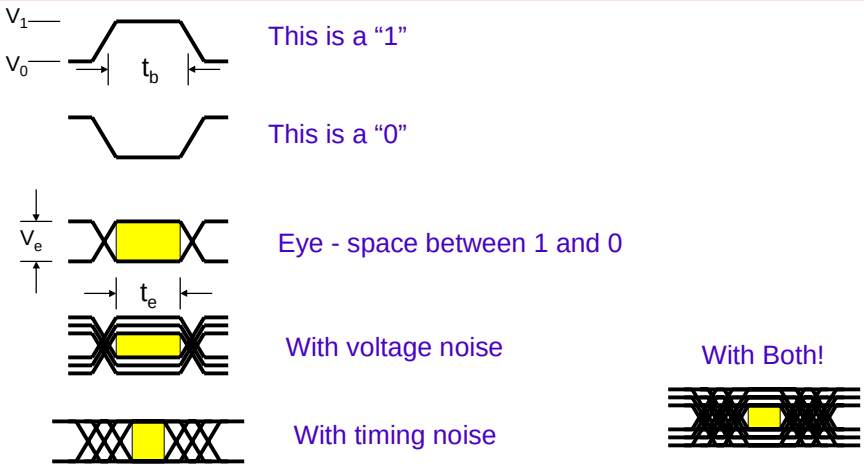
The *Eye* Diagram
A View of Noise, Signaling, and Timing



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Why is Digital Systems Engineering Important?

- System-level electrical issues are becoming more critical
  - Higher clock rates
    - wires are transmission lines
    - clock skew and jitter are a major portion of a clock cycle
    - many cables are more than one clock long
  - Lower voltages
    - more current for a given power level
    - less margin
  - Pin bottlenecks
    - need to make each signal count
- Its not just for supercomputers anymore
- Get it right or it doesn’t work

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Some Horror Stories

- A small subset:
  - >1 year chasing noise between boards in a system
  - 3 spins of an ASIC due to clock skew problems
  - periodic (daily) failures due to on-chip power supply droop
  - 6 month delay to fix faulty flip-flops
- Band-aid fixes don't work
  - a system must be designed to be robust
  - *cook-book* solutions often fail
  - what worked last time often fails
  - need to understand the problem and craft an engineering solution
- Getting it right is easy - if you think about it using the right *models*

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Some Success Stories

- Performance solutions that worked the first time
  - system-wide clock distribution with 75ps skew
  - 400Mb/s simultaneous bidirectional I/O drivers (solved a pin bandwidth problem)
  - Two-register synchronizers cut latency and synchronization failures
  - Local power regulation reduces difficulty of global distribution

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This Course Will Teach You

- To *understand* system-level electrical issues
  - understand the phenomena
  - develop engineering models for simulation and analysis
  - develop and evaluate solutions
- To design systems that work reliably the first time
  - noise budgets
  - timing budgets
- To push performance where its needed
  - signaling rates
  - synchronization latency and failure probability
  - power distribution

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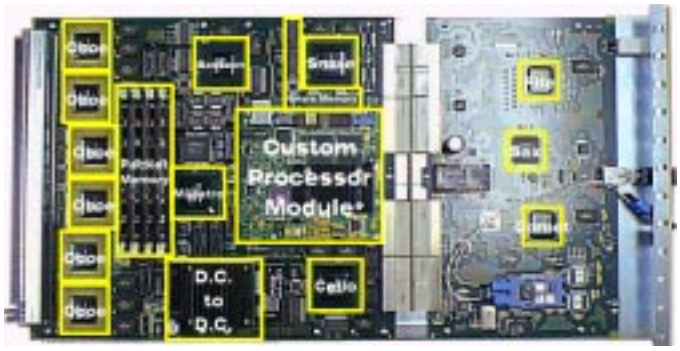
A Typical Digital System



OC-48 Line Card

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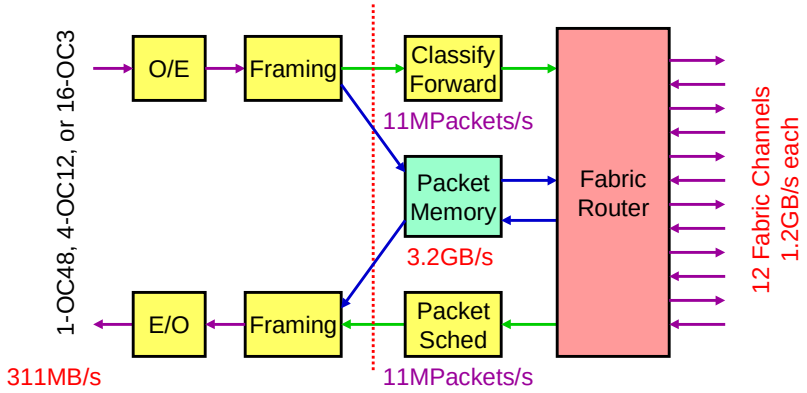
An Engineering View of this Line Card (Speeds and Feeds)



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Noise

- What is the minimum signal swing we can use reliably?
- What is the fastest rate we can signal at?
- The answer to both of these questions depends on ***noise*** and how we deal with it

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Noise Sources

- Power supply - V_{PN} = iZ = iR + Ldi/dt
- Crosstalk
- Inter-Symbol Interference
- Parameter mismatch (offset voltages)
- *Real* noise
  - thremal, shot, radiation

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Managing Noise

- Fixed v. Proportional
  - fixed noise - independent of signal swing (V_{NI})
  - proportional noise - scales with signal swing (K_N)
- Bounded v. Gaussian
  - bounded - worst-case analysis
  - gaussian - statistical analysis

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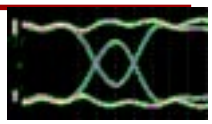
An Example Noise Calculation

- 250mV differential signal
- 15% high-frequency attenuation
- 5% crosstalk from adjacent lines
- 5% ISI from reflections
- 20mV receiver offset+sensitivity
- 10mV RMS Gaussian noise
- What is the Bit Error Rate?



Signal Swing (dp-dn)		500
Gross Margin		250
Crosstalk	0.05	25
Reflections	0.05	25
Attenuation	0.15	75
KN	0.25	125
Receiver offset+sensitivity		20
Fixed noise		145
Net Margin		105
Gaussian Noise		10
VSNR		10.5
BER		1.15E-24

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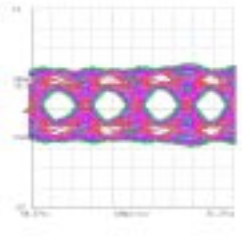
Signaling

- How to move a symbol (usually a bit) from here to there
  - how is the symbol represented?
    - "0" = -2.5mA, "1" = 2.5mA
  - how is the line terminated at each end?
    - Z_0 at both ends
  - how are references generated?
    - Differential signal
  - how does the receiver detect the symbol?
    - detect voltage across terminator



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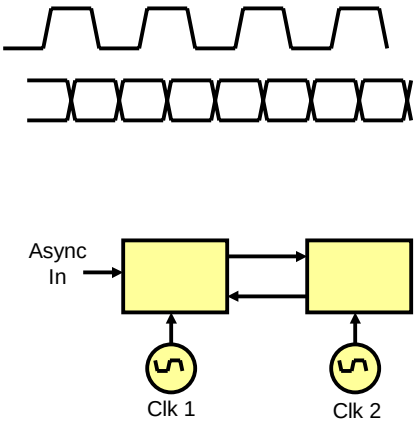
Timing and Synchronization

- How do you determine when a symbol is valid? (when a new symbol arrives?)
- Synchronous timing
  - all FFs driven by one clock
  - may be 10^5 FFs/chip 10^7 in a system
  - wires may be > 1 clock long
  - skew is a ***big*** problem
- Pipeline timing
- Self-timed design
- Multiple clock domains
  - signals must be synchronized



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Power Distribution

- Consider a system with
  - 100 20A chips (2KA)
  - A 400MHz clock (t_{ck} = 2.5ns)
  - Current can drop to zero in one clock cycle
  - di/dt = 2KA/2.5ns = _____
- What does a 1nH inductor in series with this supply current do?
- How do we solve this problem?

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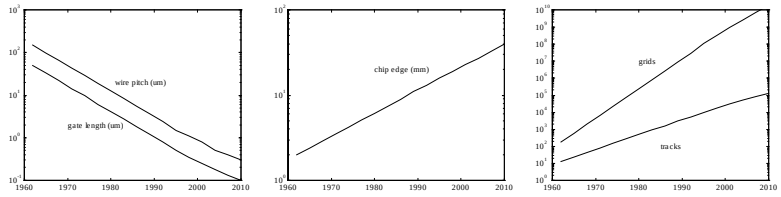
Technology Trends

- Digital systems problems are getting harder
- Moore's Law
  - grids/chip doubles every 18months (60%/year)
  - gate length shrinks by 20%/year
  - chip size increases by 20%/year



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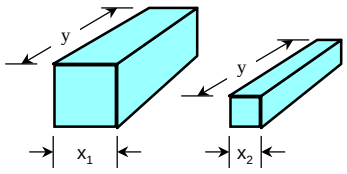
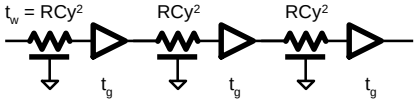
Scaling and Signaling
Wires act like 'wet noodles'



$x_2 = s\,x_1$	0.5x
$R_2 = R_1/s^2$	4x
$C_2 = C_1$	1x
$t_{w2} = R_2C_2y^2 = t_{w1}/s^2$	4x
$t_{w2}/t_{g2} = t_{w1}/(t_{g1}s^3)$	8x



$v = 0.5(t_gRC)^{-1/2}$ (m/s)	
$v_2 = v_1 s^{1/2}$	0.7x
$vt_g = 0.5(t_g/RC)^{1/2}$ (m/gate)	
$v_2t_{g2} = v_1t_{g1}s^{3/2}$	0.35x

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Scaling and Power Distribution

- Supply noise (relative to V_{DD}) doubles every year!
  - V_{DD} decreases by 20%/year
  - I_{DD} increases by 44%/year
  - f_{ck} increases by 20%/year
  - so V_{PN} = di/dt increases by 1.2^3 (73%/year)
  - and V_{PN}/V_{DD} increases by 1.2^4 110%/year!
- How do we deal with this?

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The Good News

- VLSI can be used to solve the problems it creates
- Lots of fast transistors lets us build
  - clever drivers and receivers for efficient signaling
  - on-chip regulators to simplify power distribution
  - per-line timing recovery and de-skew circuits
  - efficient synchronizers to move between clock domains
  - etc…
- In this course you will learn how to solve problems like this

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Job Security

- Digital systems problems are not static.
  - The constraints and solutions change with technology
- Beware of tried and true solutions
  - corner pin power supplies
  - edge-triggered flip-flops
  - full-swing signaling
  - just because it worked last time doesn't mean that it will still work
- The market rewards calculated risks

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Next Time

- Introduction to wires
  - electrical properties of wires
  - simple transmission lines
  - terminations and reflections
  - lossy transmission lines

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