EE273 Lecture 4
Wires Concluded
RC Lines and Measurement Techniques

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Today's Assignment

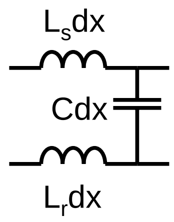
- Reading
  - Sections 6.1 through 6.3
  - Complete before class on Wednesday

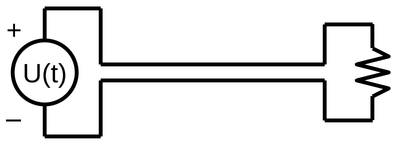
A Quick Overview

- Balanced lines
  - differential (odd) and common-mode (even) propagation
  - rise on signal is accompanied by fall on return
- Modeling wires
  - build a model to capture relevant electrical properties
  - ignore inessential elements
  - depends on rise time
- Time-Domain Reflectometer

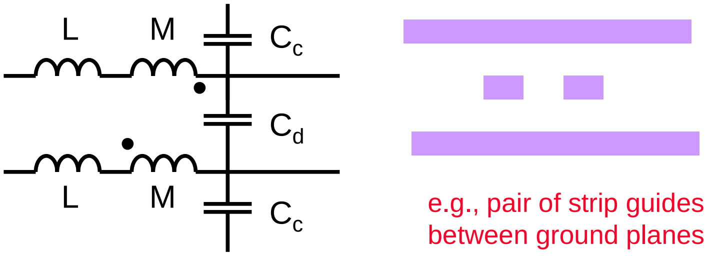
Balanced Transmission Lines

- All transmission lines have inductance in the return path
  - leads to a shift in return voltage across line
- In a balanced line, return inductance equals signal inductance
- Suppose we put a 1V step into a balanced line
  - 0.5V drop across signal inductor
  - 0.5V drop across return inductor





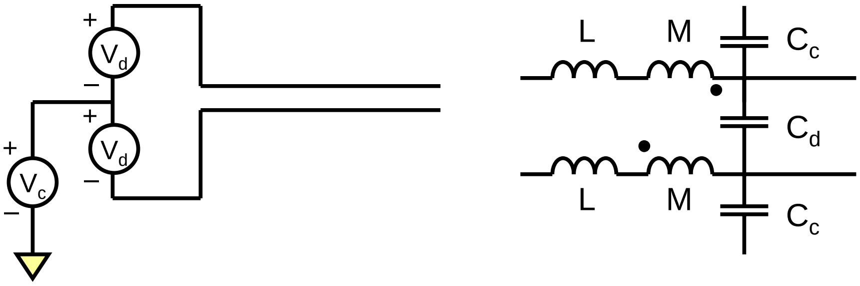
Even and Odd Mode Impedance



e.g., pair of strip guides
between ground planes

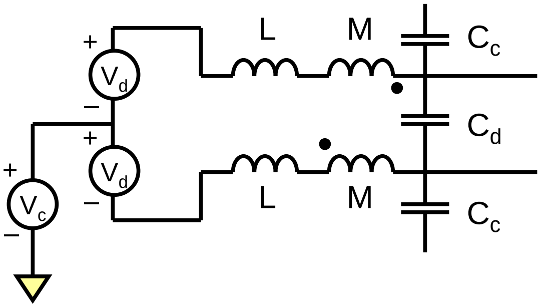
- M and C_d represent coupling between lines
- L and C_c represent coupling to other conductors

Even and Odd Mode
(Command and Differential Mode) Impedance



- Any excitation can be described as the superposition of a *differential* or *odd-mode* signal and a *common-mode* or *even-mode* signal
  - e.g. 1V step: $V_c = 0.5V$, $V_d = 0.5V$

Even and Odd Mode (Command and Differential Mode) Impedance



$$Z_D = \frac{V_D}{I_1} = \left(\frac{L-M}{C+C_D}\right)^{1/2}$$

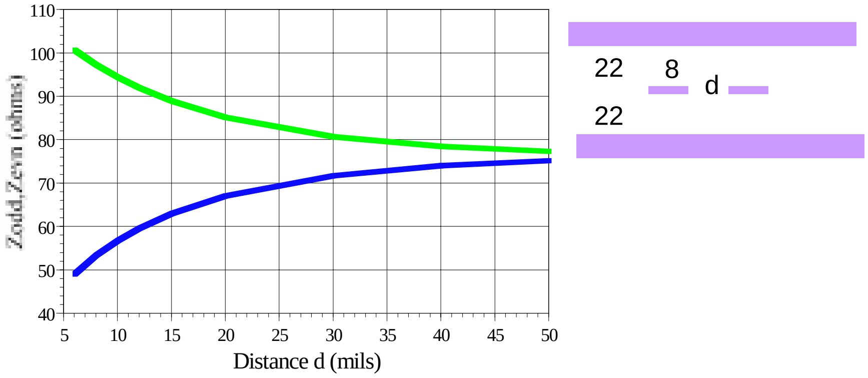
$$Z_C = \frac{V_C}{I_1} = \left(\frac{L+M}{C-C_D}\right)^{1/2}$$

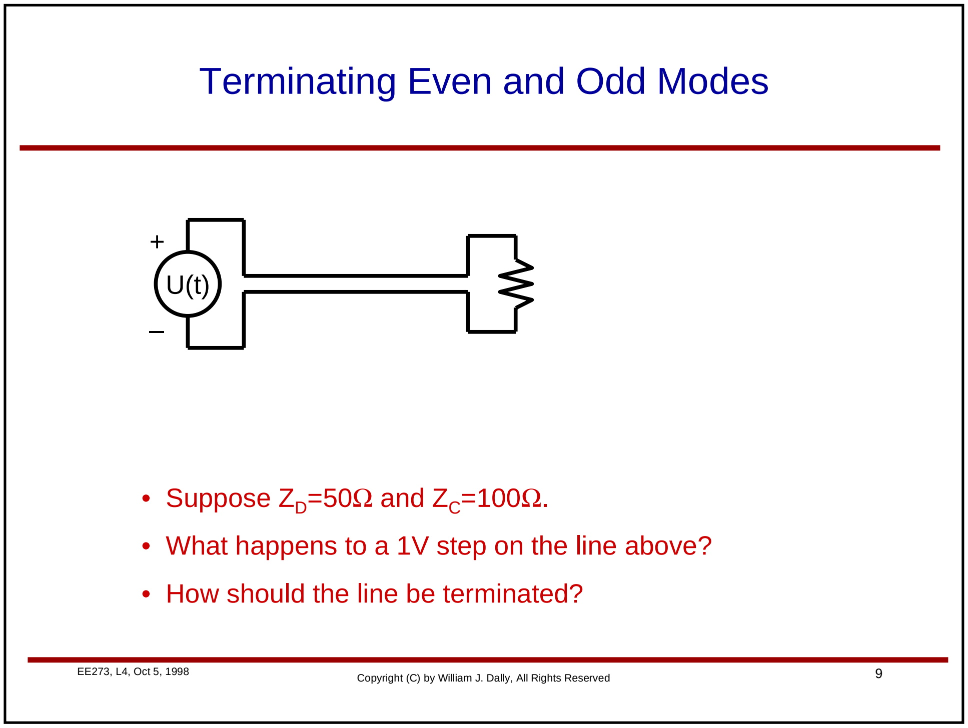
$$C = C_C + C_D$$

$$\frac{L}{M} = \frac{C}{C_D}$$

- Even and odd-mode signals see different impedance

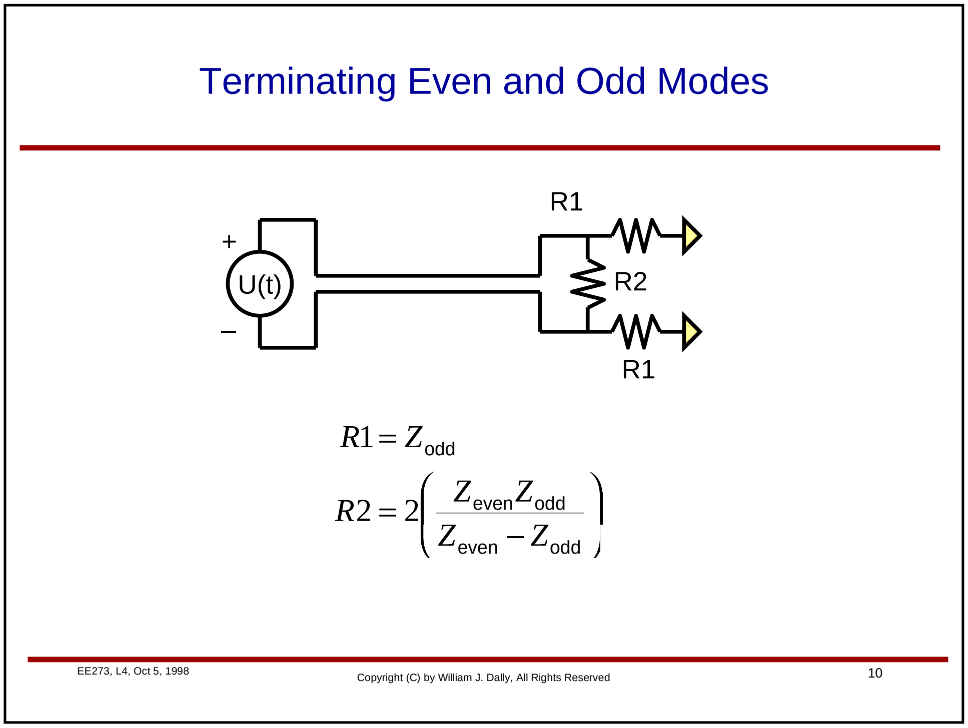
Example of Even and Odd mode impedances





Terminating Even and Odd Modes

- Suppose Z_D=50Ω and Z_C=100Ω.
- What happens to a 1V step on the line above?
- How should the line be terminated?



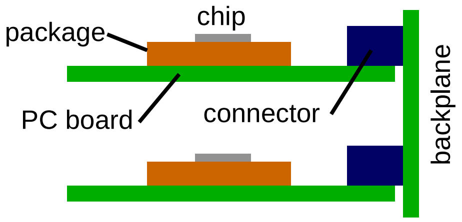
Terminating Even and Odd Modes

$$R1 = Z_{\text{odd}}$$

$$R2 = 2\left(\frac{Z_{\text{even}} Z_{\text{odd}}}{Z_{\text{even}} - Z_{\text{odd}}}\right)$$

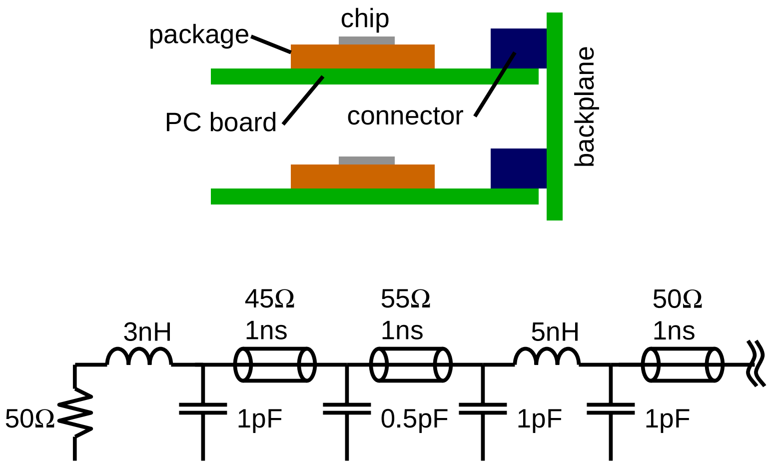
Modeling of Wires

- Given a real system
  - – chips, packages, boards, connectors, backplanes, cables
- Need to develop a *model* of the signaling medium
  - – for hand calculation of key properties
  - – for SPICE simulations
- Model must
  - – capture all *relevant* wire properties
    - transmission line properties
    - *major* discontinuities
    - terminations
  - – ignore those that are not relevant
    - e.g., short discontinuities



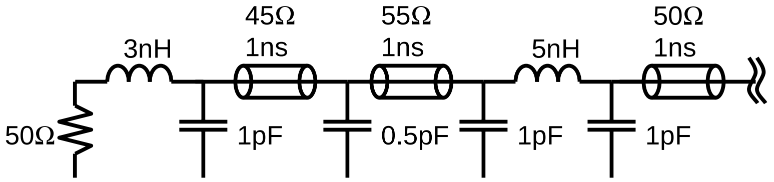
- A good model captures the *relevant* behavior while being as simple as possible

Example Model



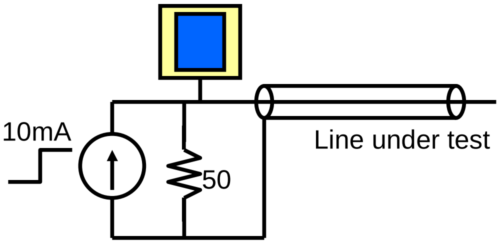
Deriving a Model

- How do we make a model of a signal path?
  - hand calculation
  - assemble models from component, connector, and package vendors
  - CAD programs
  - measurements of the actual system

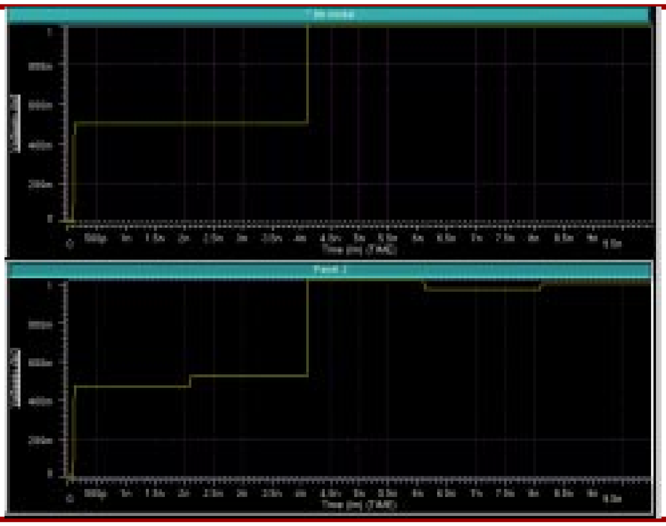


Meet the Time-Domain Reflectometer

- A time-domain reflectometer is a fast step generator and a high-speed oscilloscope.
- To characterize a line
  - inject a fast (usually 20ps) step into the line
  - observe the reflected waveform
  - what does it mean?



What made these waveforms?

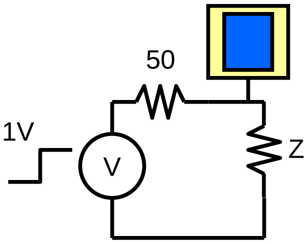


Calculating Impedance from Voltage

$$V = \frac{Z}{Z + Z_0}$$

$$(Z + Z_0)V = Z$$

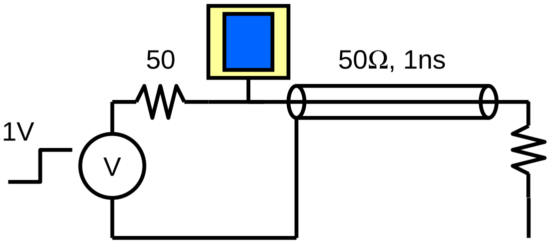
$$Z = Z_0\left(\frac{V}{1-V}\right)$$

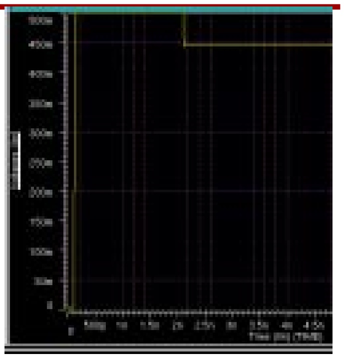


V	Z
0.50	50.0
0.47	44.3
0.53	56.4

Time of Observation is Round Trip

$$Z(x) = Z_0 \left(\frac{V(2x/v)}{1 - V(2x/v)} \right)$$

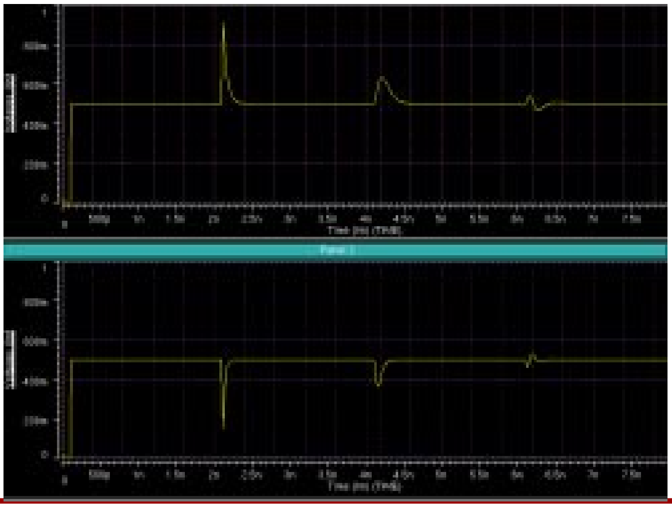




What About Inductors and Capacitors?

$$L = 2Z_0\tau_L$$

$$C = \frac{2\tau_C}{Z_0}$$



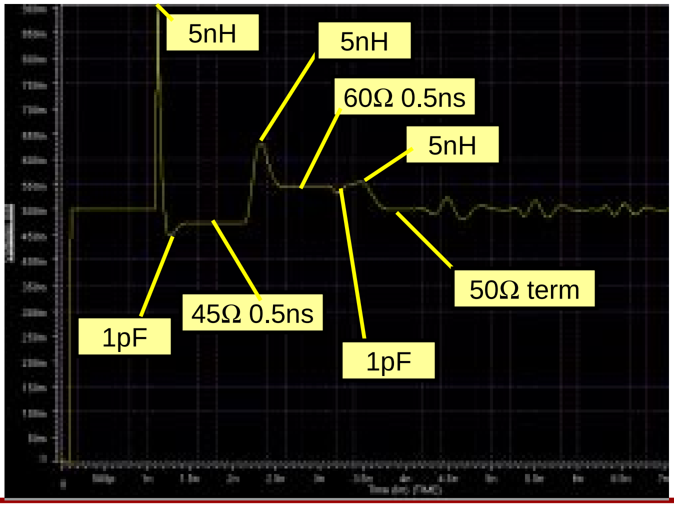
Rise-Time Degradation

- Upstream elements (Ls & Cs) low-pass the signal resulting in a longer rise-time
- This affects the reflections from down-stream elements
  - slow rising edge
  - spread out response (convolution with slow edge)
  - L & C responses don't go full swing
- This makes it
  - hard to extract exact L and C values
  - impossible to measure very small discontinuities
    - but if the TDR can't see them, neither can the signal

Extraction Procedure

- Identify regions of the TDR plot as
  - flat region - transmission line
  - bump up - inductor
  - bump down - capacitor
- Starting at source
  - determine value of Z & t, L, or C for nearest element
  - simulate to validate and determine new t_r
    - iterate as needed to get value right
  - move on to next element
- Don't need model with more resolution than your fastest rise time

Example TDR Trace


5nH

5nH

60Ω 0.5ns

5nH

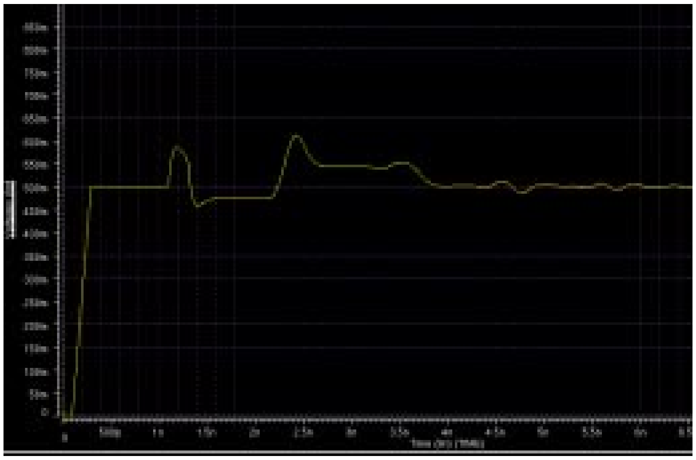
50Ω term

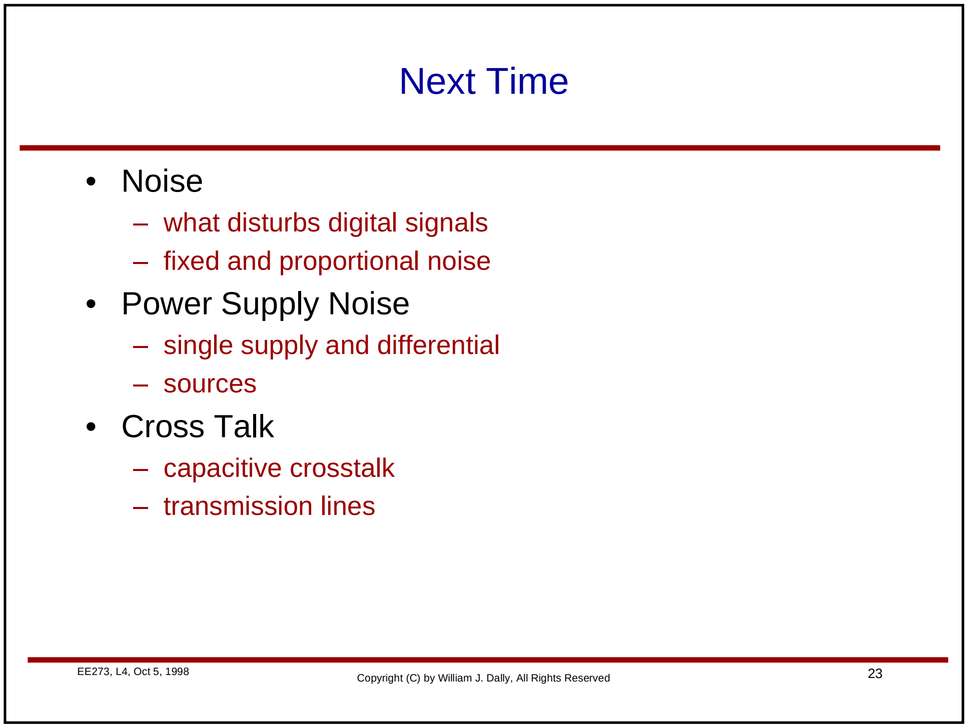
1pF

45Ω 0.5ns

1pF

Same waveform with 200ps edge





Next Time

- Noise
  - what disturbs digital signals
  - fixed and proportional noise
- Power Supply Noise
  - single supply and differential
  - sources
- Cross Talk
  - capacitive crosstalk
  - transmission lines