EE273 Lecture 8
Signaling over Lumped Media
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Today's Assignment

- Reading
  - Sections 8.1 through 8.4
  - Complete before class on Wednesday
- Reminder
  - midterm is in the evening on 10/26
  - no class on 10/26

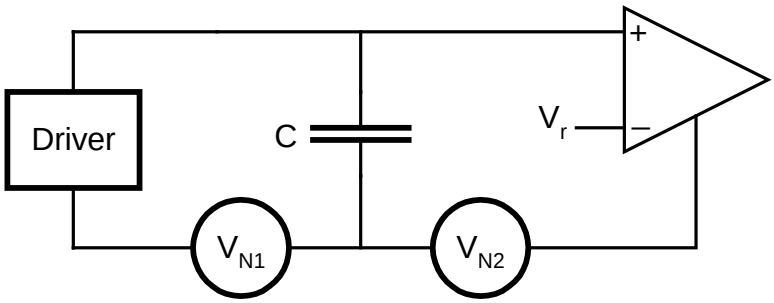
A Quick Overview

- Signaling over Capacitive Media
  - Want fast transitions and low power
  - Need to avoid supply noise
  - Current-mode signaling
  - References and Differential signaling
  - Pulsed signaling to avoid DC power dissipation
- Signaling over LRC Interconnect
  - Pin inductance and load capacitance form a tank circuit
  - Adding resistance dampens the oscillation of the tank
  - Slowing rise time reduces excitation
- Number of signal levels
  - trade off bandwidth against noise

Signaling Over Capacitive Media

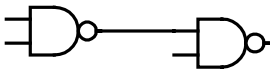
- Where do we find capacitive wires?
  - short on-chip wires with high fan-out or fan-in
    - e.g. buses, register files, RAMs
    - note that long on-chip wires are RC lines - a more difficult problem
- Desiderata
  - fast transitions
  - low power
  - these imply a small signal swing
  - to support a small swing one needs to isolate power supply noise

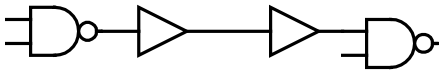
Block Diagram of Capacitive Signaling System



Conventional *Logic* Signaling

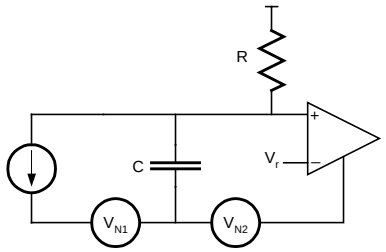
- Historically signal levels were defined to facilitate *logic circuits* not *transmission*
  - for example:
    - 0 = TGND, 1=TVDD
    - V_r=(RGND+RVDD)/2
    - slow
    - lots of power dissipation
    - no rejection of supply noise
- When transmission is a large fraction of delay, its better to switch to a representation tailored for transmission



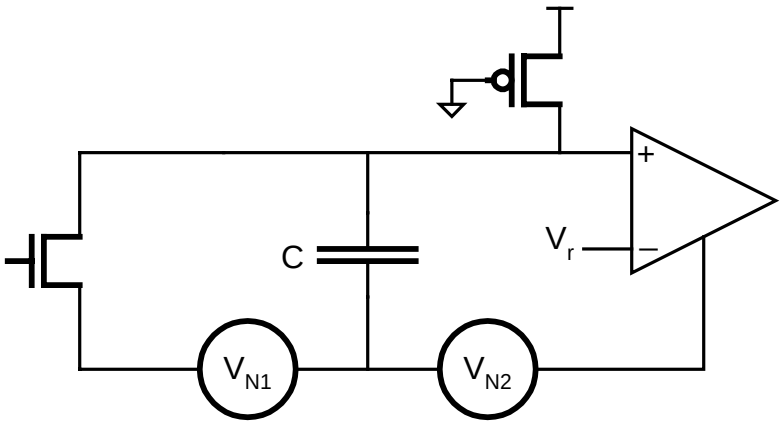


Current-Mode Signaling

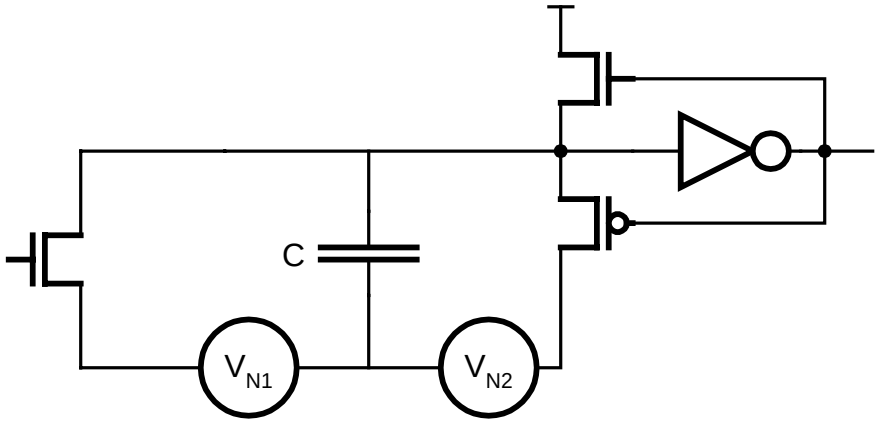
- Send logic values as small currents
  - 1=1mA
  - 0=0mA
- Detect across 'resistor' at receiver
- High Tx impedance isolates Tx supply noise
- High-pass RC removes low-frequency Rx supply noise
- Still need to generate a reference



A Current-Mode Signaling Circuit

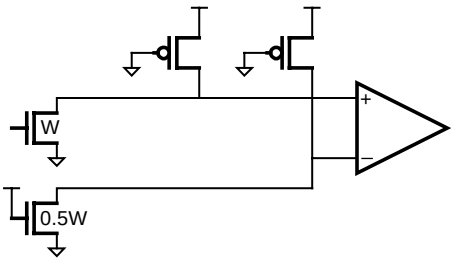


Another Current-Mode Signaling Circuit
Negative Feedback Current Sense



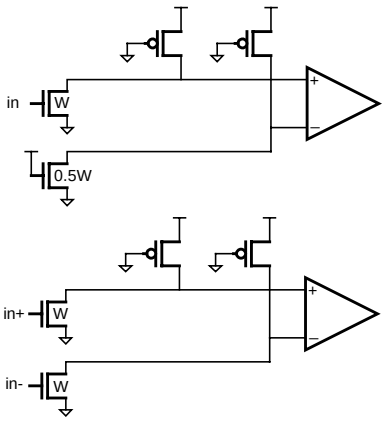
Transmitter References

- Would like to set receiver reference half-way between a ‘1’ and a ‘0’
- Simplest approach is to send half the ‘1’ current from the transmitter
  - this reference can be shared by many signals
- If drive current is 1mA, signal swing is 0.3V, and capacitance is 10pF, what is the rise time?
  - how does it depend on signal swing?



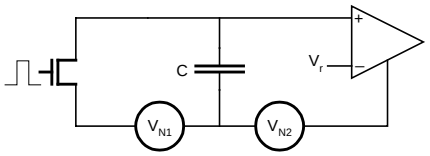
Differential Signaling

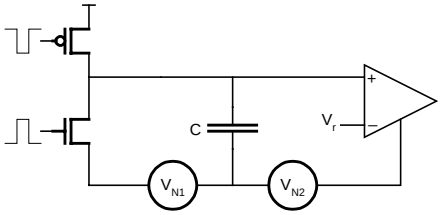
- If wire tracks are available, best noise cancellation is to send the signal and its complement
  - *twist* the signals periodically to balance crosstalk
  - better noise rejection
  - balanced load on the two lines
  - twice the signal swing for the same current (or half the rise time)
- But this still dissipates DC power!



Pulsed Signaling

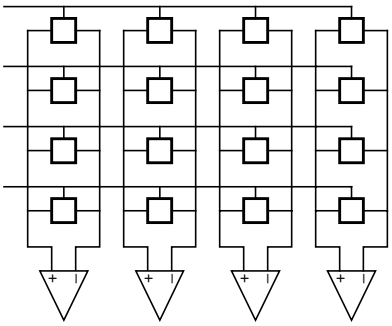
- To eliminate DC power dissipation just
  - (1) remove the 'resistors'
  - (2) drive the line with current *pulses*
- What does (1) do to noise rejection?
- How do we set the DC level of the line?
  - precharge
  - feedback
- Do we need to pulse the line in both directions?





Case Study, SRAM Bit Lines

- SRAMs have high fan-out on the word lines and high fan-in on the bit lines
- Bit lines use differential, pulsed, precharged current-mode signaling
- Typically have 50mV to 300mV swing
  - careful ground rules to make all crosstalk common mode
- Detected with clocked amplifier 10mV offset+sensitivity



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SRAM Numbers

- Typical *subarray*
  - 256 rows x 1024 columns
  - 0.5pF bit line, 2pF word line
  - on-current is 0.2mA
  - pulse width is 500ps

$$\Delta V = \frac{I\Delta t}{C} = \frac{\left(2\times10^{-4}\right)\left(5\times10^{-10}\right)}{5\times10^{-13}} = 200\text{mV}$$

- How long would it take to go full-swing?

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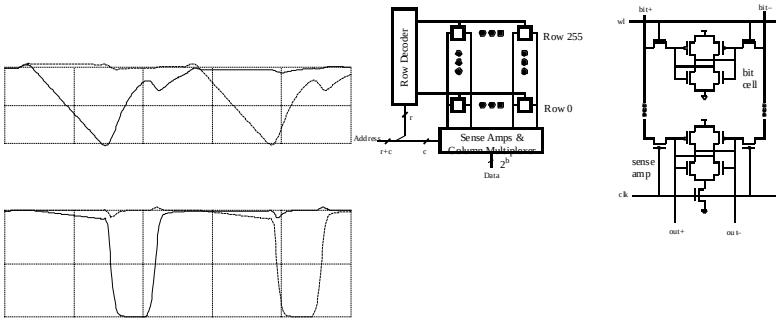
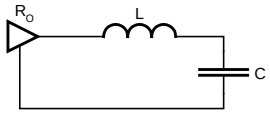
SRAM Waveforms



Signaling over LRC Interconnect
Or how not to excite the oscillator

- Short off-chip wires often look like LC tank circuits
  - inductance of package and bond wire
  - capacitance of load device
  - *long* off-chip wires look like transmission lines
- Add series or parallel resistance to dampen the oscillations
- Increase the rise time to avoid pumping energy into the LC

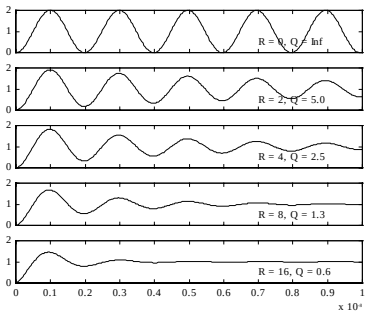


$$\omega_0 = (LC)^{-1/2}$$

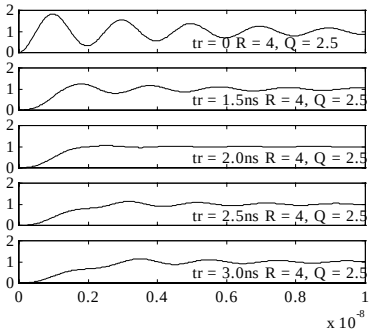
$$Q = \frac{1}{\pi R_O}\sqrt{\frac{L}{C}}$$

$$K_r = \frac{1}{\omega_0 t_r}$$

Waveforms for LRC Signaling



L=10nH, C=10pF, R from 0 to 16Ω



L=10nH, C=10pF, R=4Ω
t_r=0 to 3ns

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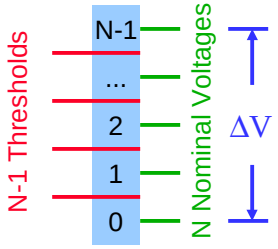
Number of Signal Levels

- There is nothing magical about 2-level or *binary* signaling
- Could use N-levels
  - N symbols
  - N nominal symbol voltages
  - N-1 thresholds
  - Nominal voltage separated from threshold by ΔV/2(N-1)



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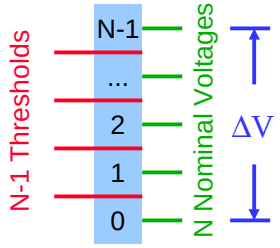
Multi-Level Signals and Noise

- In the worst case, signal can swing through ΔV, from 0 to N-1
  - proportional noise is proportional to full swing
- Gross margin is distance from nominal voltage to threshold
- Proportional noise constant, K_N must be kept very small to allow more signaling levels
- Number of bits per symbol is $\log_2(N)$



$$V_{GM} = \frac{\Delta V}{2(N-1)}$$

$$K_N \leq \frac{1}{2(N-1)}$$

Multi-Level Signals and Power

- Power per symbol (worst case) is proportional to ΔV^2
- With fixed noise sources this grows as N^2.
- So power per bit grows as

$$\frac{N^2}{\log_2 N}$$

- So why use multilevel signaling?
  - when channel is band-limited
    - it may be the *only* way to get more bits over a channel
  - when there is a very large SNR
    - so proportional noise doesn't swamp the multi-level signal.

Next Time

- Signaling wrapup
- Dealing with long on-chip RC lines
- Dealing with lossy LRC lines
- Simultaneous bidirectional signaling