CS99S
Laboratory 4 Solution

October 22, 2001

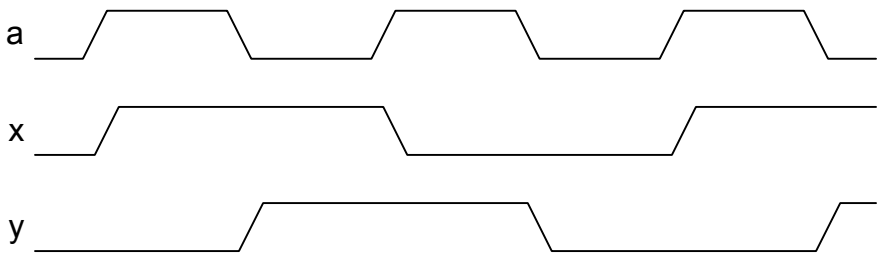
Prep Question 1: Draw the truth table (state table) for the sequential circuit with one input, a, and two outputs x and y described by the following logic equation. What does it do? Sketch the waveforms generated on x and y in response to alternating 1s and 0s on a.

$x = ((a \vee x) \wedge \sim y) \vee (\sim a \wedge x)$

$y = ((\sim a \vee y) \wedge x) \vee (a \wedge y)$

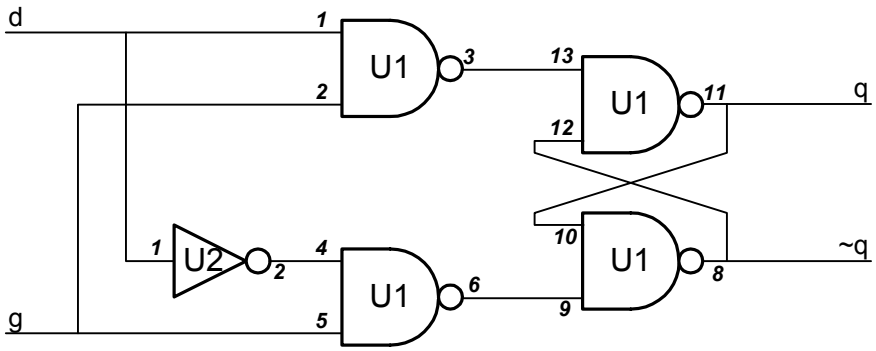
a	x	y	next x	next y
0	0	0	0	0
1	0	0	1	0
1	1	0	1	0
0	1	0	1	1
0	1	1	1	1
1	1	1	0	1
1	0	1	0	1
0	0	1	0	0

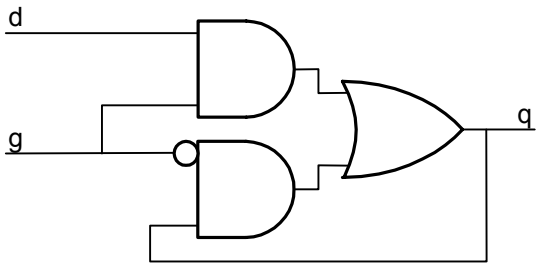
The waveforms for alternating 1s and 0s on input a are shown below:



The circuit is a 'toggle' flip-flop. The output, x, toggles on every rising edge of a and the output y toggles on every falling edge of a. With a square-wave input, this circuit generates outputs x and y with half the frequency of input a and displaced from each other by 90 degrees.

Prep question 2: Draw a schematic for a latch using only NAND gates. Label the chip numbers and pin numbers for this schematic because you are going to build it using 74AC00 chips.

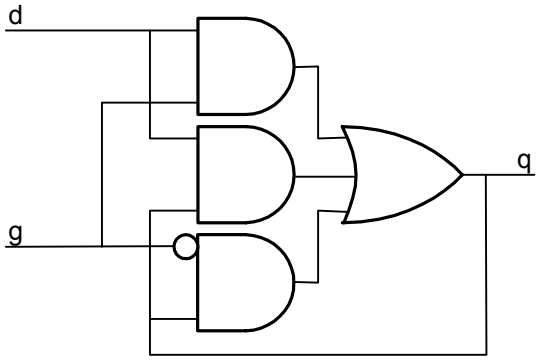




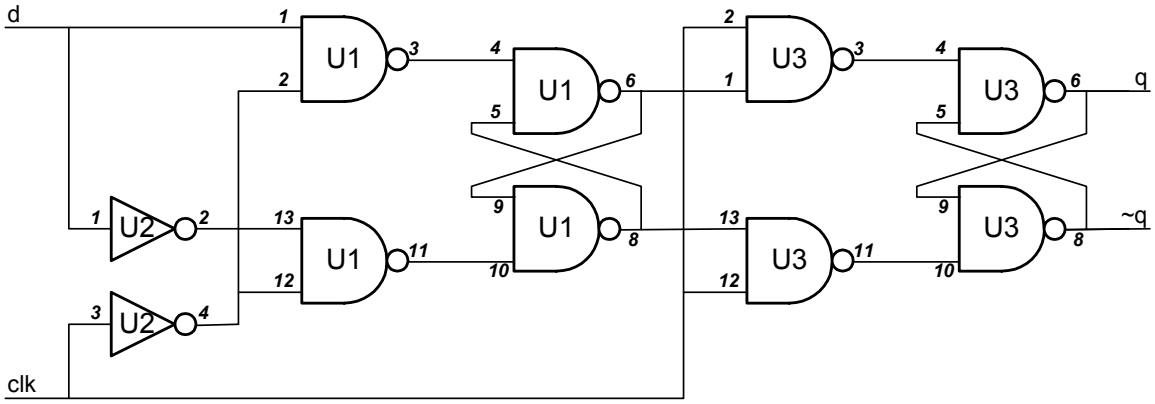
Prep question 3 (optional challenge): Explain why the latch above doesn't work and fix it. (Hint: consider what happens when g changes from high to low if the upper AND gate is much faster than the lower AND gate).

When the enable, g, changes from high to low while input d and output q are both high, the output of the upper AND gate goes low. If this happens very fast, output q may fall before the output of the lower AND gate goes high. The net result is that the "1" stored in the flip-flop is lost during this transition.

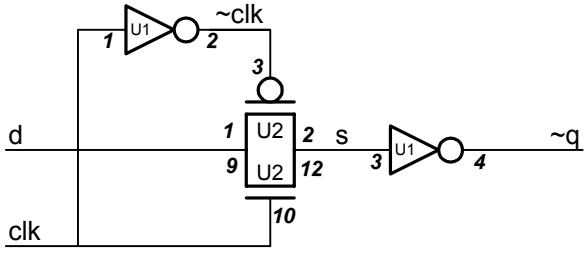
To fix the problem we add a third AND gate that holds the output high when both d and q are high regardless of the state of g as shown below. With this middle AND gate holding the output q high, the upper and lower AND gates can switch at arbitrary speeds and there is no danger of loosing the "1". This circuit is called an Earle Latch after its inventor and was widely used in high-performance computers in the 1960s and 1970s.



Prep Question 4: Starting with your schematic of a latch, draw a schematic of a D flip-flop using 74AC00 NAND gates. Number your schematic to facilitate construction.



Prep Question 5 (optional): Draw a schematic of a dynamic latch using an NFET and PFET from your 4007 and two inverters from a 74AC04. Make sure to label all unit numbers and pin numbers.



U1 74AC04 +14, -7
U2 4007 +14, -7

The Lab

Here is a photo of the D flip-flop constructed from the schematic in prep-question 4.