**CD4007C**

**Dual Complementary Pair Plus Inverter**

**General Description**

The CD4007C consists of three complementary pairs of N- and P-channel enhancement mode MOS transistors suitable for series/shunt applications. All inputs are protected from static discharge by diode clamps to \( V_{DD} \) and \( V_{SS} \).

For proper operation the voltages at all pins must be constrained to be between \( V_{SS} - 0.3V \) and \( V_{DD} + 0.3V \) at all times.

**Features**

- **Wide supply voltage range:** 3.0V to 15V
- **High noise immunity:** 0.45 \( V_{CC} \) (typ.)

**Ordering Code:**

<table>
<thead>
<tr>
<th>Order Number</th>
<th>Package Number</th>
<th>Package Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD4007CM</td>
<td>M14A</td>
<td>14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150” Narrow</td>
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<tr>
<td>CD4007CN</td>
<td>N14A</td>
<td>14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS–001, 0.300” Wide</td>
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</table>

*Note: Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.*

**Connection Diagram**

**Note:** All P-channel substrates are connected to \( V_{DD} \) and all N-channel substrates are connected to \( V_{SS} \).
### Absolute Maximum Ratings (Note 1)

- **Voltage at Any Pin**:
  - $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$

- **Operating Temperature Range**:
  - $-40°C$ to $+85°C$

- **Storage Temperature Range**:
  - $-65°C$ to $+150°C$

- **Power Dissipation ($P_D$)**
  - Dual-In-Line: 700 mW
  - Small Outline: 500 mW

- **Lead Temperature (Soldering, 10 seconds)**: 260°C

- **Note 1**: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

### DC Electrical Characteristics

#### Symbol: $I_L$
- **Parameter**: Quiescent Device Current
  - **Conditions**: $V_{DD} = 5.0V$
  - **Limits**: Min: 0.005 µA, Typ: 0.05 µA, Max: 0.5 µA

#### Symbol: $P_D$
- **Parameter**: Quiescent Device Dissipation
  - **Conditions**: $V_{DD} = 5.0V$
  - **Limits**: Min: 2.5 µW, Typ: 25 µW, Max: 75 µW

#### Symbol: $V_{OL}$
- **Parameter**: Output Voltage LOW
  - **Conditions**: $V_{DD} = 5.0V$
  - **Limits**: Min: 0, Typ: 0.01 V, Max: 0.05 V

#### Symbol: $V_{OH}$
- **Parameter**: Output Voltage HIGH
  - **Conditions**: $V_{DD} = 5.0V$
  - **Limits**: Min: 4.95 V, Typ: 5.0 V, Max: 4.95 V

#### Symbol: $V_{INL}$
- **Parameter**: Noise Immunity (All inputs)
  - **Conditions**: $V_{DD} = 5.0V, V_O = 3.6V$
  - **Limits**: Min: 1.5 V, Typ: 1.5 V, Max: 1.4 V

#### Symbol: $I_{iN}$
- **Parameter**: Output Drive Current
  - **Conditions**: $V_{DD} = 5.0V, V_O = 0.4V, V_I = V_{DD}$
  - **Limits**: Min: 0.35 mA, Typ: 0.3 mA, Max: 1.0 mA

#### Symbol: $I_{iP}$
- **Parameter**: Output Drive Current
  - **Conditions**: $V_{DD} = 5.0V, V_O = 2.5V, V_I = V_{SS}$
  - **Limits**: Min: -1.3 mA, Typ: -1.1 mA, Max: -0.9 mA

#### Symbol: $I_i$
- **Parameter**: Input Current
  - **Conditions**: Any Input
  - **Limits**: Min: 0, Typ: 0, Max: 4.5 µA

### AC Electrical Characteristics (Note 2)

**$T_A = 25°C$ and $C_L = 15 pF$ and rise and fall times = 20 ns. Typical temperature coefficient for all values of $V_{DD} = 0.3%/°C$**

#### Symbol: $t_{PLH}$
- **Parameter**: Propagation Delay Time
  - **Conditions**: $V_{DD} = 5.0V$
  - **Limits**: Min: 35 ns, Typ: 75 ns

#### Symbol: $t_{PLH}$
- **Parameter**: Transition Time
  - **Conditions**: $V_{DD} = 5.0V$
  - **Limits**: Min: 50 ns, Typ: 100 ns

#### Symbol: $C_i$
- **Parameter**: Input Capacitance
  - **Conditions**: Any Input
  - **Limits**: Min: 5 fF, Typ: 5 fF

**Note 2**: AC Parameters are guaranteed by DC correlated testing.
AC Test Circuits

Switching Time Waveforms
Physical Dimensions inches (millimeters) unless otherwise noted

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150° Narrow
Package Number M14A
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