

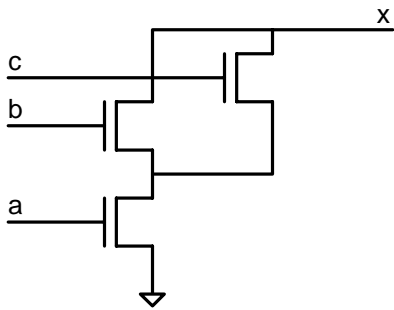
CS99S

Laboratory 2 Solution

Copyright © W. J. Dally 2001

October 17, 2001

Prep question 1: Draw an NFET network that connects the output to 0 when a AND (b OR c) is true ($a \wedge (b \vee c)$ in shorthand).



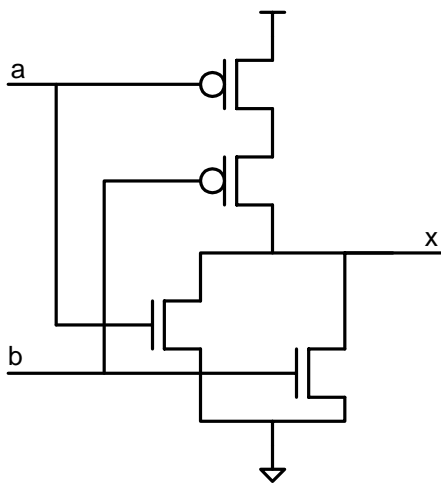
Prep question 2: Write down the normal form and simplify the equation for the following truth table.

a	b	x
0	0	1
0	1	1
1	0	0
1	1	0

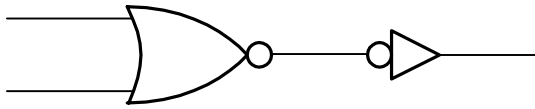
Normal form: $x = (\sim a \wedge \sim b) \vee (\sim a \wedge b)$

Simplified: $x = \sim a$

Prep question 3: Sketch a transistor diagram for a 2-input NOR gate.

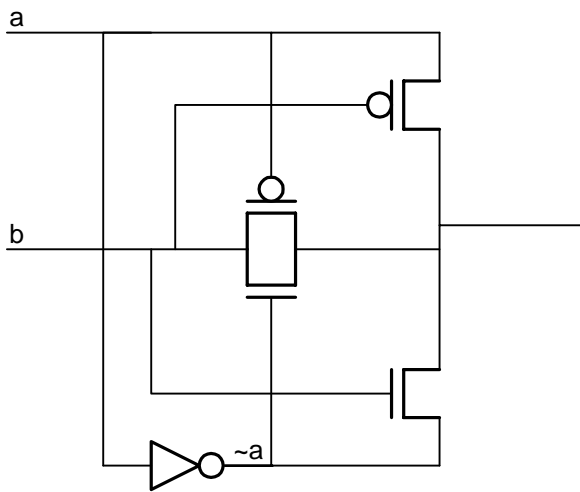


Prep question 4: Show how to create an OR gate by composing inverting gates.

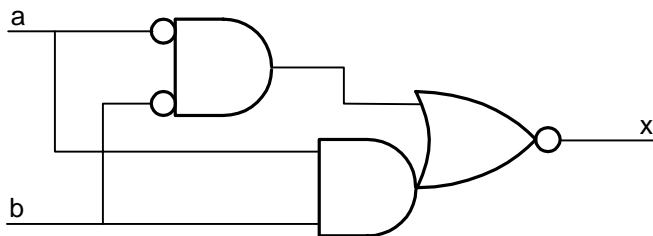


Prep question 5 (optional challenge question): Sketch an implementation of an XOR gate using NFETs and PFETs. A prize goes to the solution with the minimum number of transistors.

The best solution I am aware of takes six transistors. Kudos to Jason Payne and Derek Gaw for finding this solution.

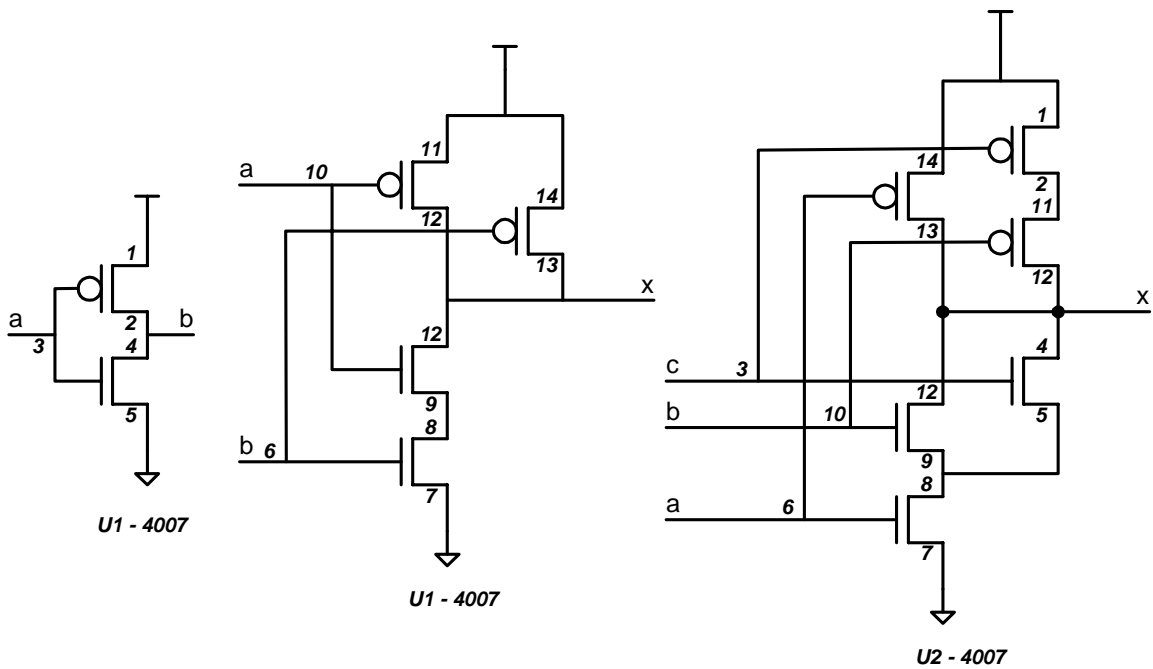


It turns out that this solution is not used much in practice because it does not *restore* the signal levels on inputs a and b – passing the input signal level directly through to the output. The smallest design that restores signal levels takes 10 transistors four in a NOR gate and six in an and-or-invert gate.



Lab:

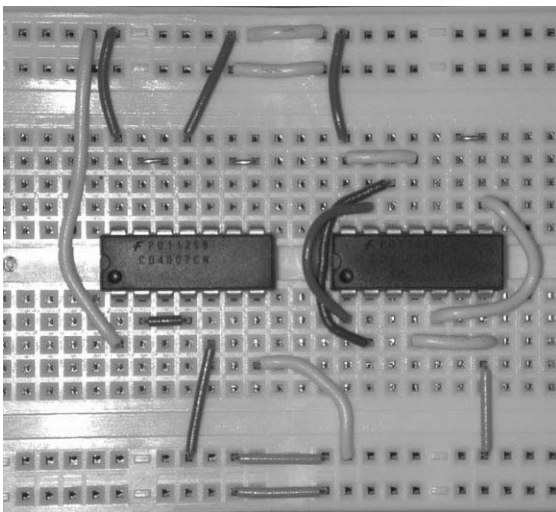
In preparation for the lab, sketch how you will wire up these gates using the CD4007. Specifically, draw a schematic showing the pins used by the source, gate, and drain of each transistor.



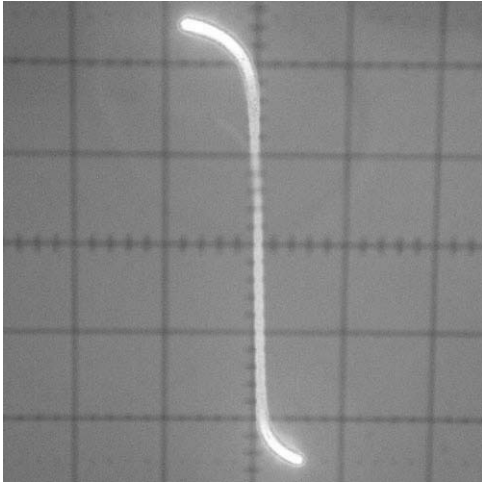
Once you wire up these three gates, you will evaluate each of them using the following three steps.

1. Verify their logical operation using switch inputs and an LED as output.
2. Trace the DC transfer curve – input voltage vs. output voltage for at least one of your gates.

Here's the wiring for lab 2. The two CD4007s are placed in a row and connected to Vdd and GND on pins 14 and 7 respectively. All wires are cut to length and all wiring is laid flat against the board. No wiring is done over the chips. Note the use of bare wire jumpers between adjacent pins.



Here is the transfer curve measured from my inverter. The scale is 1V per division on both axes. The center of the screen is in = 2.5V, out = 2.5V.



3. Observe the AC transfer curve – input and output waveforms vs time.

Here's the AC response – 50ps per horizontal division. The very sharp waveform (2V/division scale) is the input from the 74AC14 wired as an oscillator. The ringing is due to the poor quality of the power supply wiring on our breadboards. The sloppy looking trace (1V/division) is the output of my inverter.

