

CS99S

Laboratory 7 Wiring Table

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Chip	Input	Signal	Chip Pin	From Pin	Comment
ROM, U1	a[0]	carB	U1-8	DIPSW-1	Input DIP Switches
	a[1]	carA	U1-7	DIPSW-2	
	a[2]	Function	U1-6	DIPSW-3	
	a[3]	pc[0]	U1-5	U3-14	Program Counter
	a[4]	pc[1]	U1-4	U3-13	
	a[5]	pc[2]	U1-3	U3-12	
	a[6]	pc[3]	U1-2	U3-11	
	a[7]	pc[4]	U1-1	U4-14	
	a[8]	pc[5]	U1-23	U4-13	
	a[9]	pc[6]	U1-22	U4-12	
	a[10]	pc[7]	U1-19	U4-11	
	~we	VDD	U1-21	VDD	Control Signals
	~oe	GND	U1-20	GND	
	~ce	GND	U1-18	GND	
VDD	VDD	U1-24	VDD	Power Supplies	
GND	GND	U1-12	GND		
DFF, U2	d[0]	GND	U2-3	GND	Data Inputs
	d[1]	d[0]	U2-4	U1-9	
	d[2]	d[1]	U2-7	U1-10	
	d[3]	d[2]	U2-8	U1-11	
	d[4]	d[3]	U2-13	U1-13	
	d[5]	d[4]	U2-14	U1-14	
	d[6]	d[5]	U2-17	U1-15	
	d[7]	d[6]	U2-18	U1-16	
	~ce	d[7]	U2-1	U1-17	Clock Enable
	cp	CLK	U2-11	Clock Osc	Clock
VDD	VDD	U2-20	VDD		
GND	GND	U2-10	GND		
PC-L, U3	p[0]	GND	U3-3	GND	Parallel Load Inputs
	p[1]	d[0]	U3-4	U1-9	
	p[2]	d[1]	U3-5	U1-10	
	p[3]	d[2]	U3-6	U1-11	
	~sr	~reset	U3-1	DIPSW-4	Reset DIP Switch
	~pe	~d[7]	U3-9	U5-2	Load command
	cep	VDD	U3-7	VDD	Always count
	cet	VDD	U3-10	VDD	
	cp	CLK	U3-2	Clock Osc	Clock
	VDD	VDD	U3-16	VDD	

	GND	GND	U3-8	GND	
PC-H, U4	p[0]	d[3]	U4-3	U1-13	Parallel Load Inputs
	p[1]	d[4]	U4-4	U1-14	
	p[2]	d[5]	U4-5	U1-15	
	p[3]	d[6]	U4-6	U1-16	
	~sr	~reset	U4-1	DIPSW-4	Reset DIP Switch
	~pe	~d[7]	U4-9	U5-2	Load command
	cep	VDD	U4-7	VDD	Always count
	cet	tc	U4-10	U3-15	
	cp	CLK	U4-2	Clock Osc	Clock
	VDD	VDD	U4-16	VDD	
GND	GND	U4-8	GND		

Inverter, U5	a[0]	d[7]	U5-1	U1-17
	VDD	VDD	U5-14	VDD
	GND	GND	U5-7	GND

5 spare inverters - pins 2-6, 8-13.

LEDs

Agreen	q[6]	U2-16
Ayellow	q[5]	U2-15
Ared	q[4]	U2-12
Bgreen	q[3]	U2-9
Byellow	q[2]	U2-6
Bred	q[1]	U2-5

And here's what it looks like when you're done:

