

Signal Integrity Considerations for 10Gbps Transmission over Backplane Systems



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This presentation will show the results of work done in joint collaboration between Teradyne Connection Systems, Inc. and AMCC.

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Teradyne - Tom Cohen - Tom is currently a principle mechanical engineer in the New Product Development group. His current activities include the design and analysis of high speed next generation products. During Tom's 15+ years of industry experience he has received numerous interconnect patents and has authored several papers. Tom has a BS degree in Mechanical Engineering from the University of Pittsburgh .

Teradyne – Gautam Patel - is currently a signal integrity engineer in the New Product Development group. He performs measurements, modeling, and simulation of backplane interconnects. His other functions include applications support, technical presentations and writing of technical papers. Gautam has an MS in Electrical Engineering from Northeastern University.

AMCC - Jeff Smith -Jeff is currently managing the Marketing Applications Board Design Group at AMCC. The group produces OC-48 to OC-192 Evaluation Board designs for AMCC's new chipsets. His specialization is in Signal Integrity, High Speed Digital Design and PCB/MCM Technology. Background includes over 20 years in Electro Optic Sensors, Fiber Optic System Designs and Applications.

MSEE - Electro-Optics from University of Washington 1984

BSEE – Systems from Michigan State University 1980

Agenda

- Scope
- High Speed Connectors
- PCB Termination
- Laminates
- Passive System Measurements
- Active System Measurements
- Conclusions, future work



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Scope:

This paper will focus on the elements that comprise the signal path in copper backplane system to determine the effects of running point to point differential signals at speeds up to 12 GB/s.

The elements considered in this study include trace topology, laminate material, high speed backplane connectors, and the launch effects due to the plated through via.

The elements will be individually characterized through measurements, then combined and measured as a passive system. The intent is not to provide a detailed study on any of the elements, but rather to reduce the variables in the system for a first cut at the most promising combined solution.

Finally, OC-192 devices were added to the system to both take measurements on a realistic fully active system and determine the performance gains provided by the chip set through means such as CDR. The information gained will be useful in future efforts to optimize 10 GB/s systems, but also to provide design guidelines at lower data rates.

Backplane Connectors

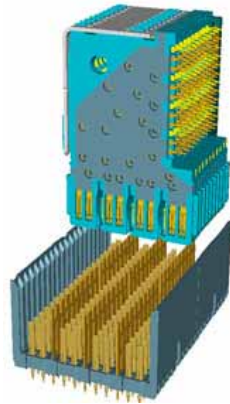


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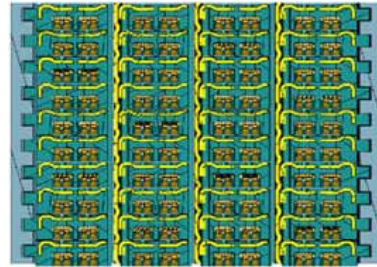


The connectors used in this study are both internally shielded, 100Ω matched impedance connectors designed for backplane systems. Measurements will be shown for both the Teradyne HSD and Teradyne GbX connectors. The intent is not to do a detailed connector comparison, but rather to characterize high speed systems with two high performance differential connectors. Because connector density can be a constraint in backplane system design, the representative interconnects selected also had to have a high density of real signals (signal pairs after ground assignments). The measured HSD connector provides thirty-eight real pairs per inch while GbX provides fifty-five real pairs per inch.

Mating Interface Cross Section



GbX™
Cross Section Mating Interface



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The electrical characterization of a high speed connector is typically reported as interpair crosstalk and connector/launch impedance.

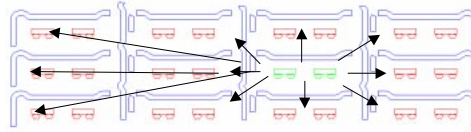
In typical backplane application the connector is seen at least twice by the signal as it passes from card to card, and therefore must not excessively attenuate the signal.

Any connector intended for highspeed design will need low multipin crosstalk in spite of a need for a high density interface. GBx achieves these requirements by closing each signal pair in a shielded box through the mating interface.

For more information see your local Teradyne Rep or visit the Teradyne web site at www.tcs.teradyne.com

Connector Crosstalk

Multiline, BXT



$T_r = 80\text{pS}$	
VHDM-HSD™	4.3%
GbX	3.1% to 4.2%

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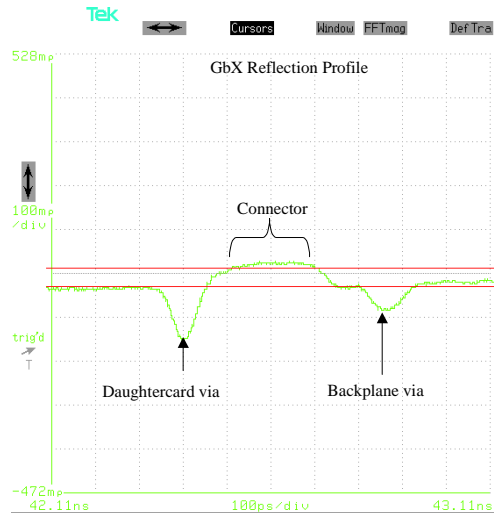
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The multipair crosstalk is reported as voltage induced the worst case victim pair in the grid with all neighboring pair being simultaneously excited. In the case of GBx the values include 11 simultaneously switching pairs

Connector Reflections

$T_r = 80\text{pS}$	
VHDM-HSD™	6%
GbX	2.5%



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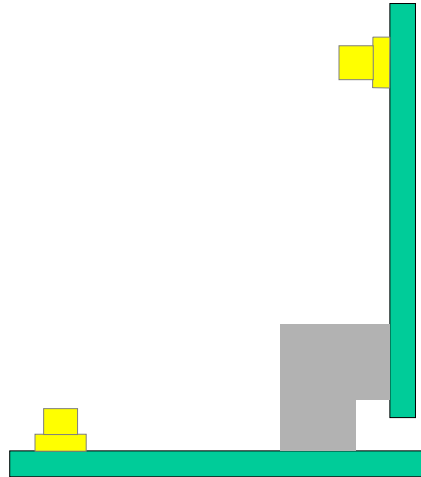
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Reflective energy loss due to excessive connector reflections would be detrimental in a system. The measurements include the capacitive disruption of the via's and the connector. Connector impedance is measured on a TDR while mounted to a suitable set of test boards. Reflection is calculated from the peak values on the TDR in the connector region. Connector reflections are shown in Slide 8.

The via capacitive effect will be treated separately in the next section with measurements for both standard and tuned holes. The plated through hole performance is dependent on a number of variables including ground plane clearance and card thickness.

SINGLE CONNECTOR TEST FIXTURES

UNCOUPLED



-FR-4 BOARD MATERIAL
(BACKPLANE)

-LOW LOSS MATERIAL
(DAUGHTERCARD)

-3 in. TRACE LENGTHS
(DAUGHTERCARD AND
BACKPLANE)

-8 mil LINE WIDTHS

-0.080" CARD THICKNESS

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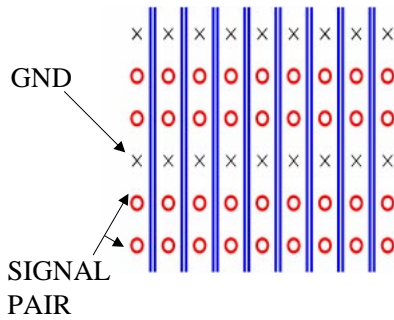
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Single Connector Test Vehicle

The GbX test fixture used to determine single connector performance was configured with eight mil, uncoupled transmission lines, standard board launch (0.0236in. drill, 0.0356in. pad, 0.0476 anti-pad), and a three inch path length on both the daughtercard and backplane. Laminate material was limited to FR-4 and a high-speed material with a loss tangent of approximately 0.004.

Recommended PCB Routing



COMPLIANT PIN

	FHS	Pad	Anti-Pad	STND Trace
GbX	0.018"	0.036"	0.048"	0.008"
HSD	0.022"	0.040"	0.052"	0.008"



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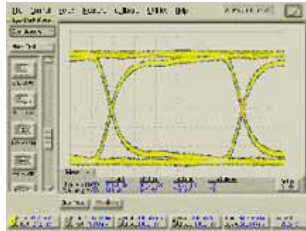
The geometry specific to various connectors influence the launch into the printed circuit boards (PCB's). The pin density and via diameter limit the maximum trace width that can route out of or through a footprint. For high speed transmission, signal traces need an adequate cross section to limit copper losses. Compliant pin termination is the predominate method to terminate contacts in backplane systems due to the difficulty in uniformly soldering the large thermal mass of the backplane. (Also providing the ability for single pin repair.) The compliant pin boards were used in testing for this study, with both standard and varied ground plane clearances.

The maximum line width and spaces listed provide 100Ω differential impedance and are listed on slide 5 for each family. Trace widths the test fixtures were .008" unless otherwise noted. Subsequent sections will vary line width.

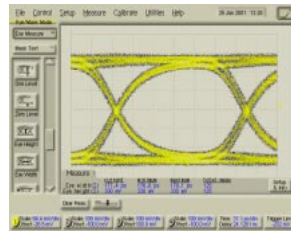
The standard plated through hole diameter for both connectors are also listed for compliant pin version of the connectors. For the GbX launch, the plated through hole capacitance is reduced by using an 0.018" compliant pin in conjunction with a special anti-pad. The capacitance can be further reduced by using various methods such as counter-boring or dual-density drilling. Some of these variations will be shown in the system test measurement section to follow.

Single Connector Eye Patterns

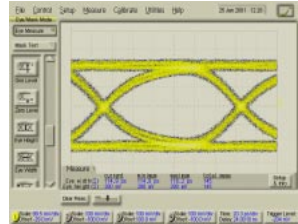
2.5Gbits/sec



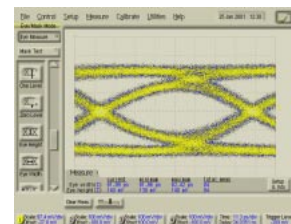
5.0Gbits/sec



7.5Gbits/sec



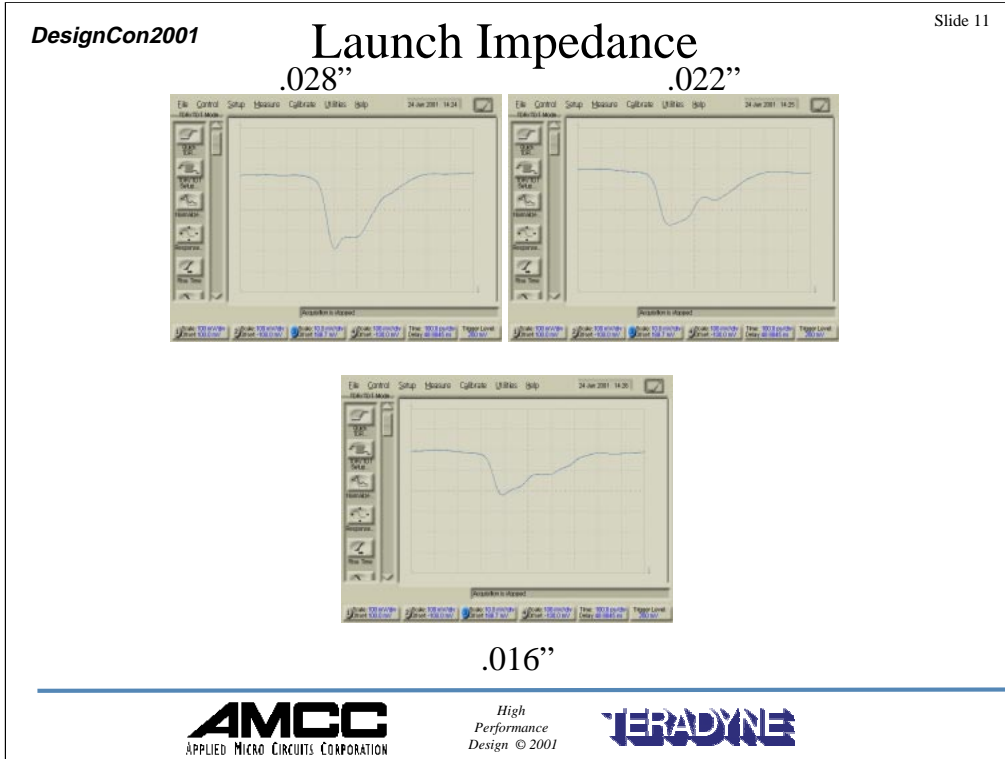
12.0Gbits/sec



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The data on slide 10 demonstrates connector performance at 2.5 Gbits/sec through 12 Gbits/sec. Single connector performance has been characterized by traditional methods such as reflections, crosstalk, and eye patterns. The measured data will be carried forward into the improved passive system.



BOARD LAUNCH:

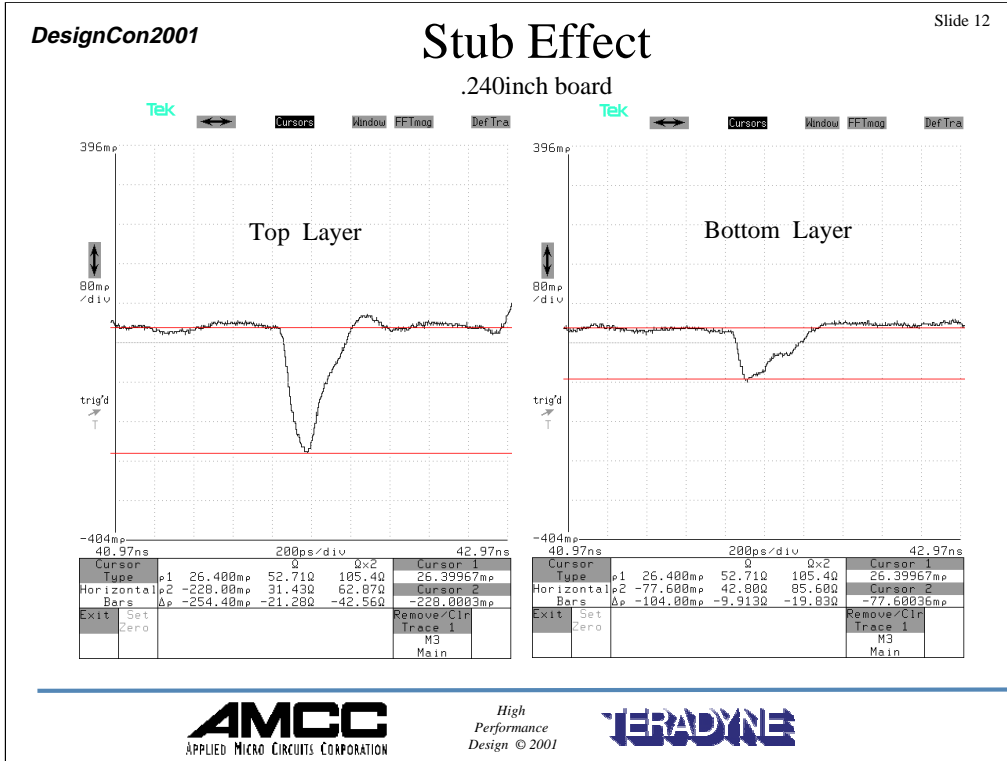
The connector launch is a factor in reaching data rates of up to 10 Gbits/sec. Currently, there are two common types of connector launches, the pad/via type and plated through hole. Because of manufacturing limits due to plating of through vias a pad/drilled via combination has been shown to have a similar lump capacitance value when compared to a reduced diameter PTH for backplane applications. (Design Con 2000)

When a pad is added to this hole, even a very small pad, the added surface capacitance can make the launch look electrically like a larger hole size without a surface pad.

It has been shown (Teradyne DesignCon 2000) that reducing the diameter of the plated through hole diameter of the plated through hole diameter in PCBs reduces the amount of excessive capacitance in the hole which allows for a better impedance match. Slide #11 illustrates the effect of reducing the diameter of a plated through hole.

Because any launch has some inductance, the launch impedance has proven to be a better indicator of performance than simple lump capacitance value.

Other launch alternatives are currently available such as laser drilled micro vias and buried vias. Although electrical models show these to be promising, this first cut testing will not include these more exotic technologies.

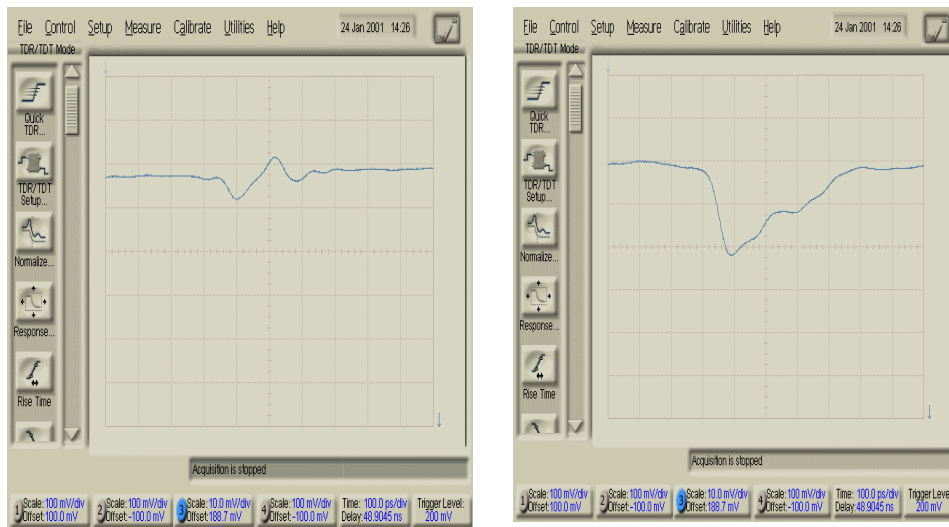


STUB

In signal launch terminology, the “stub-effect” is denoted as the resonant effect created when a trace enters a hole on a top layer of the board and leaves the hole on another top layer, creating a length of unused hole in the board which is left to ring, and create an effective decrease in impedance. An example of stub effect can be seen in slide #12.

A reflection profile is shown of two plated through holes on the same board at raw TDR rise times. The holes are exactly the same except for the length of metal stub on the launch. The first hole has approximately 0.220in. of stub and the second launch has approximately 0.010in. of metal stub. The impedance mismatch is greater for the maximum stub with an impedance of 31.43 Ohms compared to an impedance of 40.65 Ohms.

Expanded Clearance



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Expanded Ground Clearances

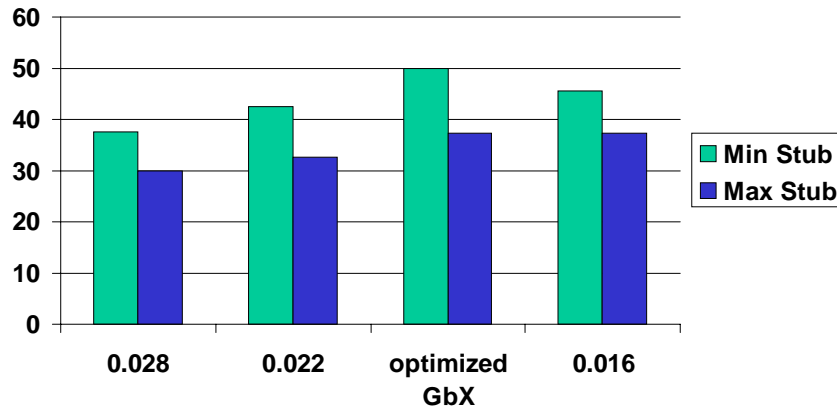
Another way to improve PCB hole impedance is to expand the anti-pads in the ground planes of the boards. Enlarging the clearances reduces the effective capacitance between inner ground clearances and the barrel of the plated through holes.

Slide 15 shows the improvement in the time domain produced by enlarging the anti-pads on a standard hole.

Counter Bore

Counter boring effectively reduces the capacitive effect of plated through holes by making the printed circuit board look electrically thinner (any removed portion of the plated through hole decreases the amount of anti-pad to barrel capacitance generated) and reduces the stub effect.

Measured PTH Impedance Summary



* 0.240" board thickness

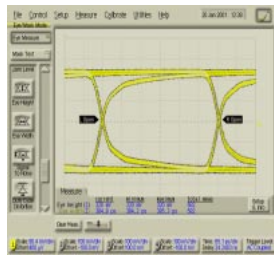
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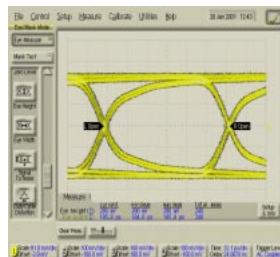
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From the data measured, an improved impedance matched hole can be produced using current technologies. By decreasing the diameter of the plated through hole, reducing the amount of unused hole, removal of non-functional pads (Design Con 2000), and increasing the anti-pad diameter, the reflections are reduced and signal attenuation is minimized.

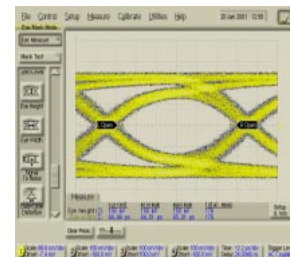
Laminate Only Tests FR-4 vs. Low Loss Laminate



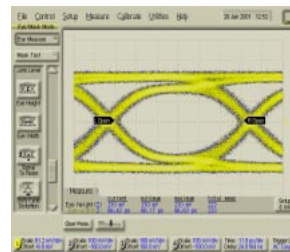
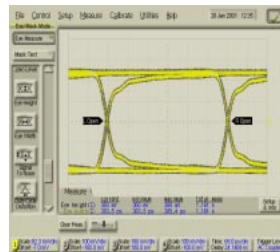
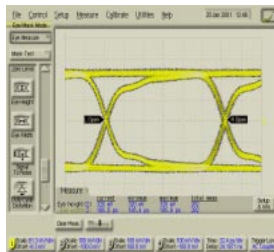
2.5 Gbits/sec



5.0 Gbits/sec



12.0 Gbits/sec



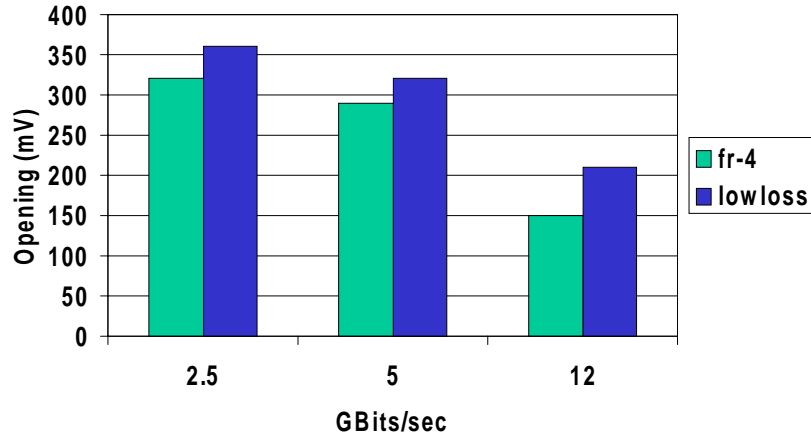
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Laminate selection is another variable to be considered in designing a 10 Gbits/sec system. In this case study, two materials will be considered. The traditional material (FR-4) and a more exotic laminate with a lower dielectric constant and reduced loss tangent. Both test fixtures had an equal number of layers and identically layouts (trace topologies, minimal stubs, improved SMA launch) with thickness variations caused only by changes in material thickness to get a fifty ohm transmission line. Board thickness was approximately 0.80in. and trace length was limited to 6 in. At 2.5 Gbits/sec rates differences between materials and line widths, may be small, but as speeds approach 10 Gbits/sec even incremental line length changes begin to show measurable differences.

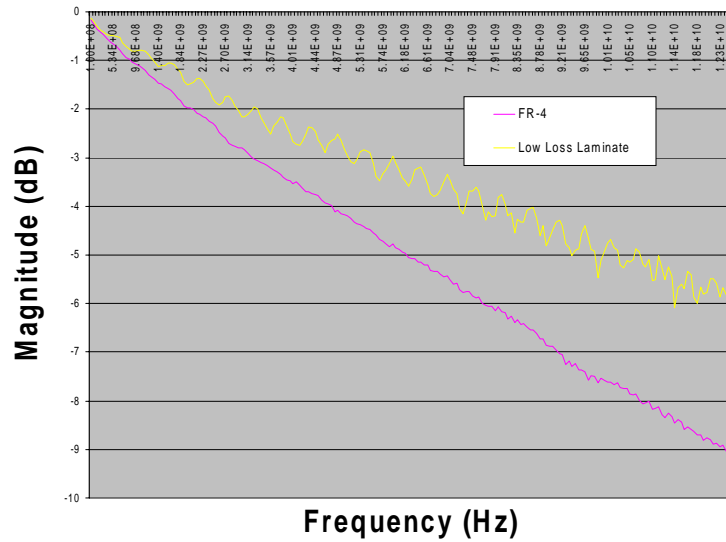
Opening vs Data Rate



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S21, FR-4 vs. Low Loss Laminate



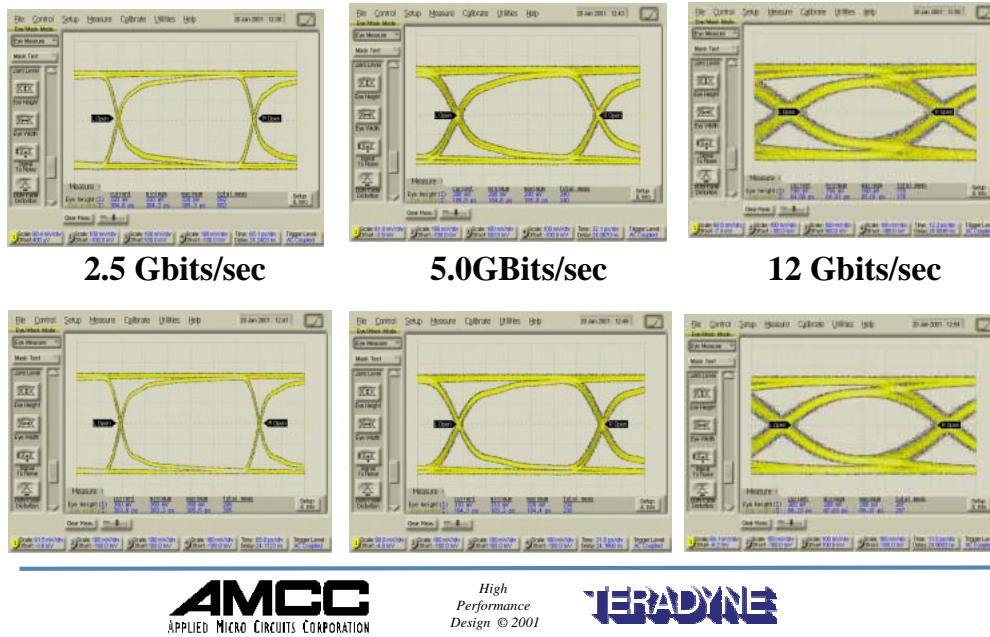
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MATERIALS

From measured data, it can be shown that traditional materials attenuate the signal more than the exotic laminates at high rates. At 12 GBits/sec the exotics offered over a 15% improvement in eye opening (see slides 15 and 16). And at the fifty percent power point offered over 2GHz in additional bandwidth (see slide 17).

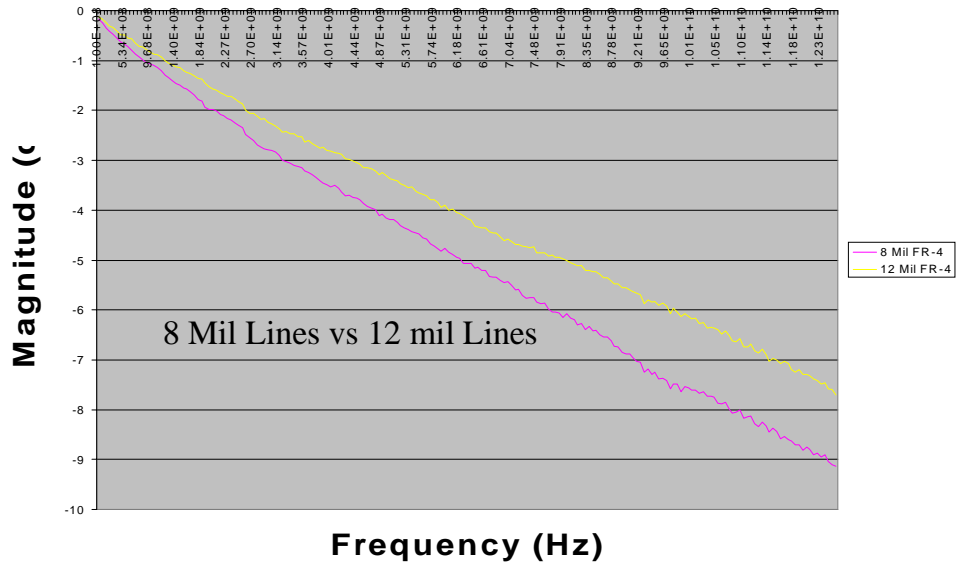
8 mil Lines vs 12 mil Lines



WIDTHS

Two line widths were evaluated using the aforementioned fixtures 8 & 12 mils. Both widths were in FR-4 and the data measured at low data rates showed little difference. At 12 Gbits/sec 12 mil offered a 10% improvement over 8 mils (see slide 18), which translated into over a 1 GHz in bandwidth at the fifty percent power point (see slides 19).

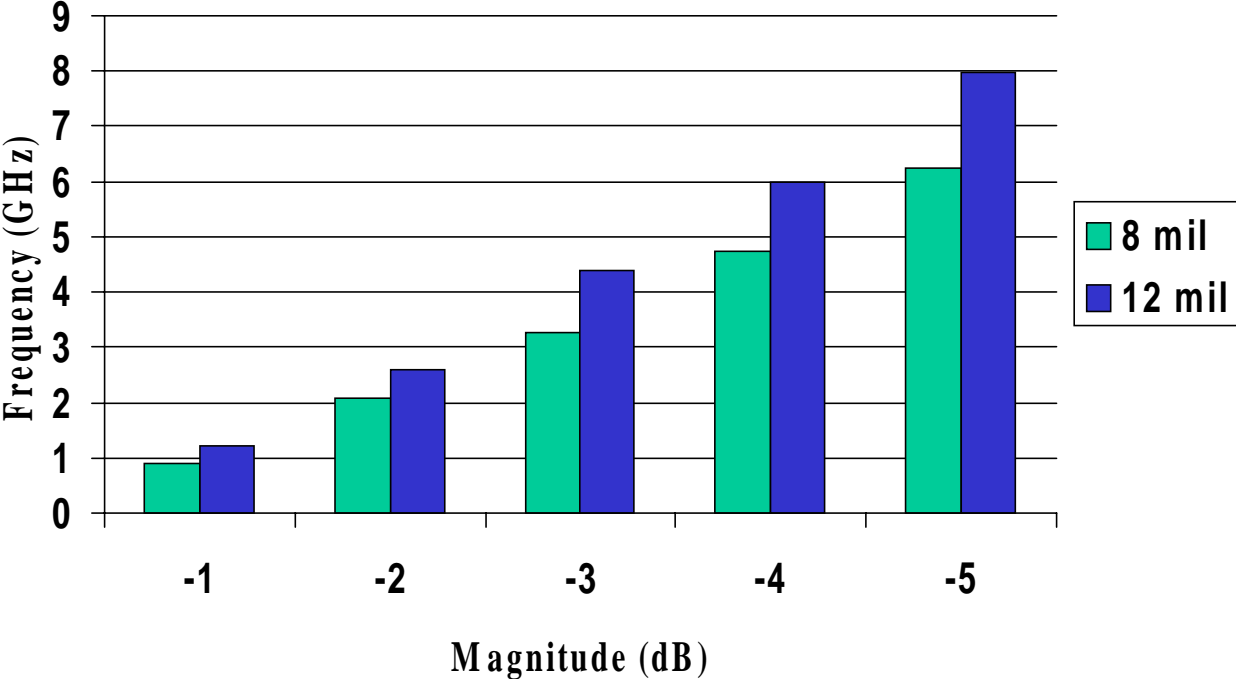
Additional materials and line widths will be considered in the passive system.



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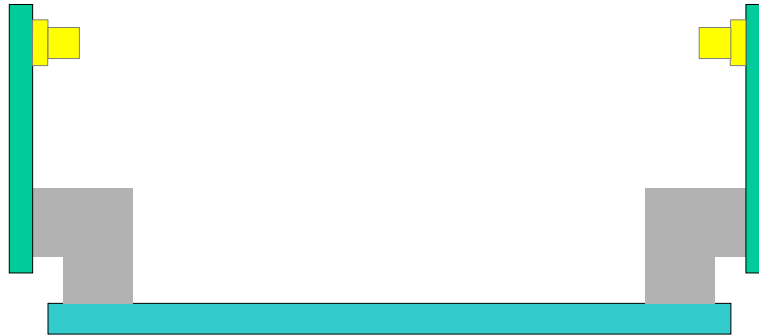


Line Width vs Loss



PASSIVE SYSTEM TEST FIXTURE

- Low Loss Daughtercards
(3 in. TRACE LENGTHS, 8 mil LINES, ~0.080" THICK)
- Low Loss Backplane
and 10 in. TRACE LENGTHS, 8 and 12 mil LINES, ~0.120" THICK)



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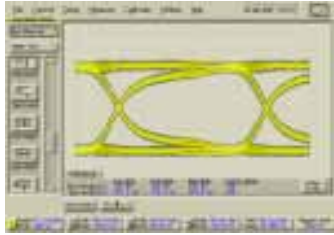
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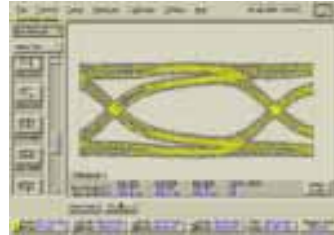
The optimized passive system test fixture consisted of two low loss daughtercards ($\sigma \sim 0.004$) with uncoupled eight mil transmission lines, non-standard plated through hole signal launches, and a three inch path length. The backplane used was constructed out of a low loss material ($\sigma \sim 0.004$) with coupled eight and twelve mil transmission lines, non-standard board launches, five and ten inch trace lengths.

11in Passive System

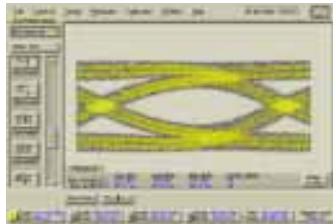
2.5G bits/sec



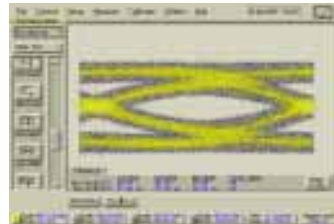
5.0G bits/sec



7.5G bits/sec



10.0G bits/sec

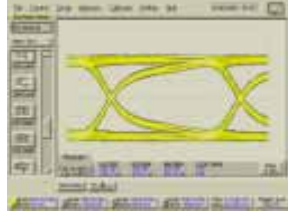


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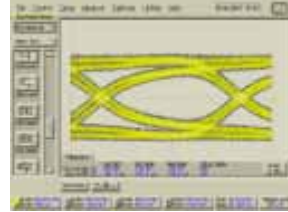


16 in Passive System

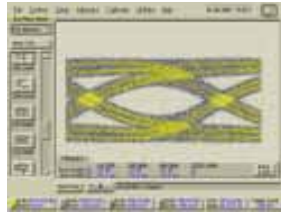
2.5Gbits/sec



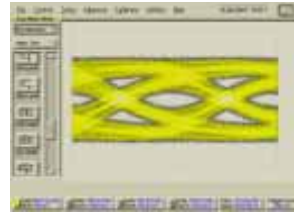
5.0Gbits/sec



7.5Gbits/sec



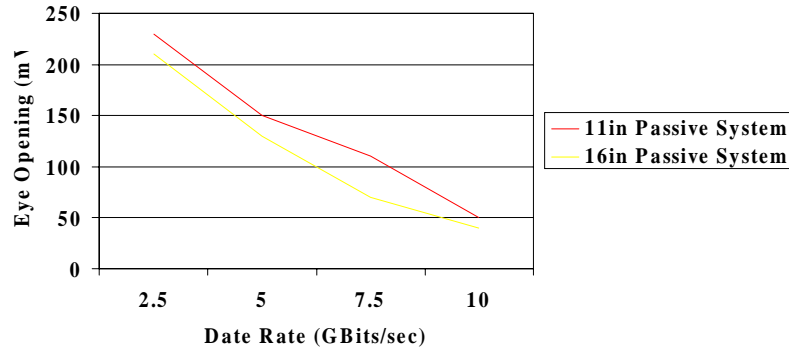
10.0Gbits/sec



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Eye Opening vs Data Rate



* Opening measured with oscilloscope eye measure mode

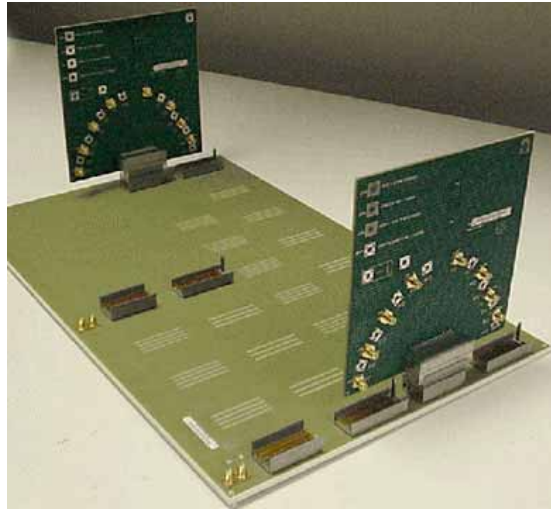
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An eye opening of seventeen percent of its original value (85mV) can be achieved at path lengths up to sixteen inches. The measured system utilized all of the optimized parameters discussed in this paper (large trace widths, small diameter plated through holes, non standard anti-pads, and a high speed differential connector). In an integrated system design, all components must be optimized to achieve system performance (bandwidth) at data rates in excess of 10Gbits/sec. With rates increasing in 4X increments - traditional design rules must be rewritten and incorporated with other anomalies that will occur in a system designed for these speeds.

Standard Passive Backplane System



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In this section we will be looking at the characteristics of the passive backplane system with standard clearances, no attempt to reduce stub length, or any of the other modifications done in the previous optimize passive backplane section. The passive backplane system consists of a backplane made from different material and trace lengths with two mated backplane connectors. Essentially the signal will be passed from one daughtercard through the connector, backplane and then through another connector and out through a SMA connection.

A picture of one of the passive backplane systems with SMA connector daughter cards are shown in the picture above.

Passive Backplane Evaluation Grid

Trace Length	Backplane Material					
	FR4	Getek	Rogers	LD621	Nelco 13	Nelco 6000SI
5"				GbX		
10"	HSD	HSD	HSD/GbX	GbX		
20"	HSD	HSD	HSD/GbX			
40"	HSD	HSD			HSD/GbX	HSD/GbX

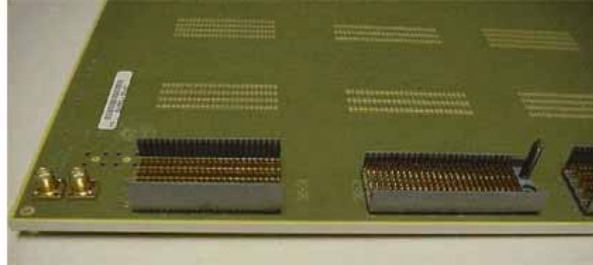


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The various backplane material, trace length and connectors that will be evaluated are shown in the slide above. For all the passive system test a 2e23 pseudo-random pattern length was used with a 500mV swing. The backplanes were approximately 0.2" thick and had 8 mil lines and spaces for a 100 Ohm differential impedance. The daughter cards were routed single ended, 50 Ohm impedance, and were approximately 0.1" thick. The HSD daughter card incorporates the non-circular clearance similar to that used on the backplane. This is shown in the next slide. The GbX daughter card does **not** use the non-circular clearance, instead a standard circular clearance was used. This will result in data that will not be as good as if the non-circular clearance had been used.

VHDM-HSD and GbX Backplane Routing

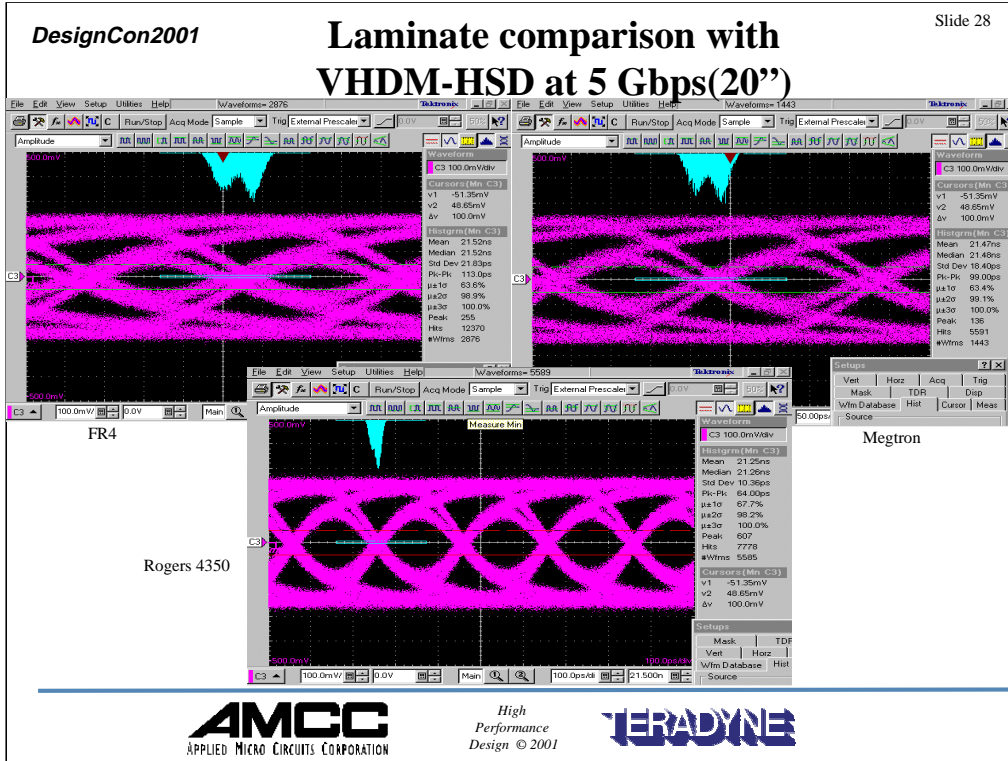


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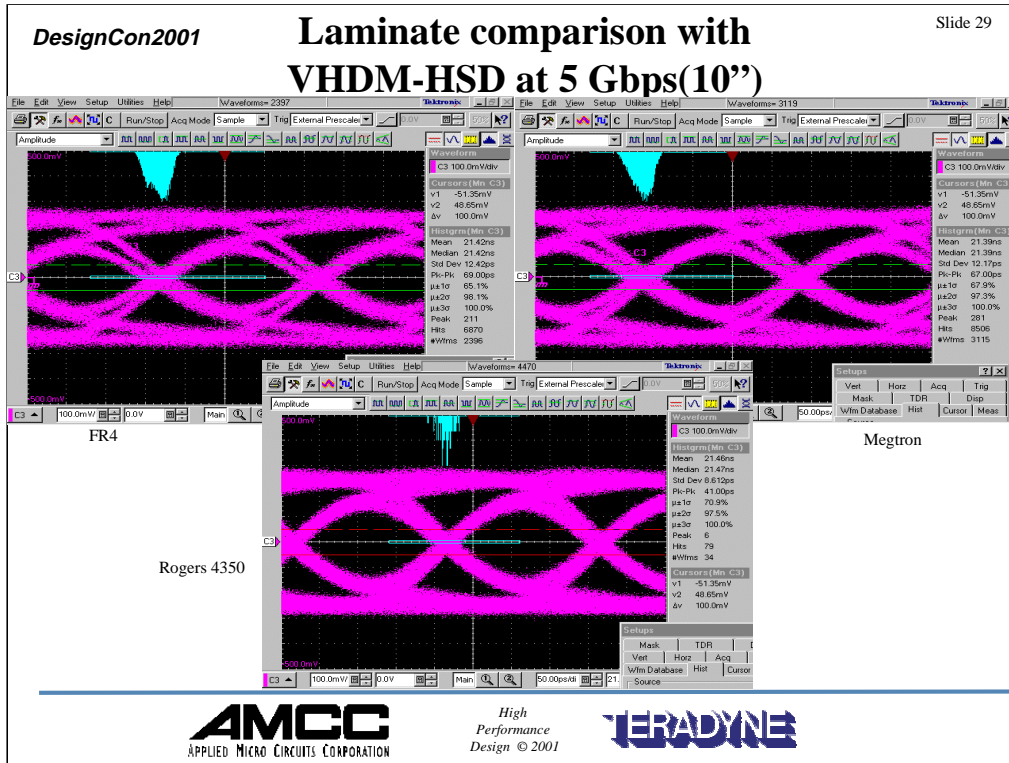
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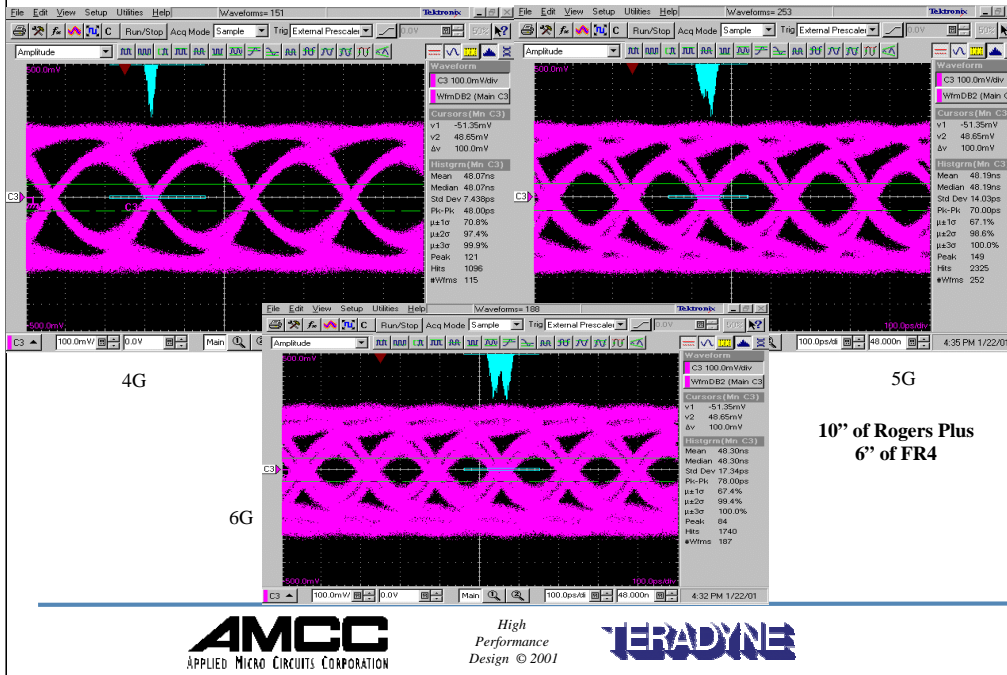
From the figure above the routing for GbX is very similar to HSD.



The first analysis was done with a 20" trace length and FR, Megtron and Rogers with the HSD 8 row connector at a data rate of 5 Gbps. The eye-patterns in the picture above is organized in the following fashion, FR4 top left, Megtron top right and Rogers bottom middle. The Rogers 4350 is clearly the best performer of these three materials. It provides 49ps of less jitter (113ps vs. 64ps) and nearly 100mV of additional eye-opening (60mV vs. 160mV) than FR4.



The next analysis was done with a 10" trace length in FR4, Megtron and Rogers with the HSD 8 row connector at a data rate of 5 Gbps. The eye-patterns in the picture above is organized in the following fashion, FR4 top left, Megtron top right and Rogers bottom middle. The Rogers 4350 is clearly the best performer of these three materials. It provides 49ps of less jitter (69ps vs. 41ps) while all the materials had >100mV of eye-opening. This shows that the system performance at 10" has less sensitivity to laminates as it does at 20"

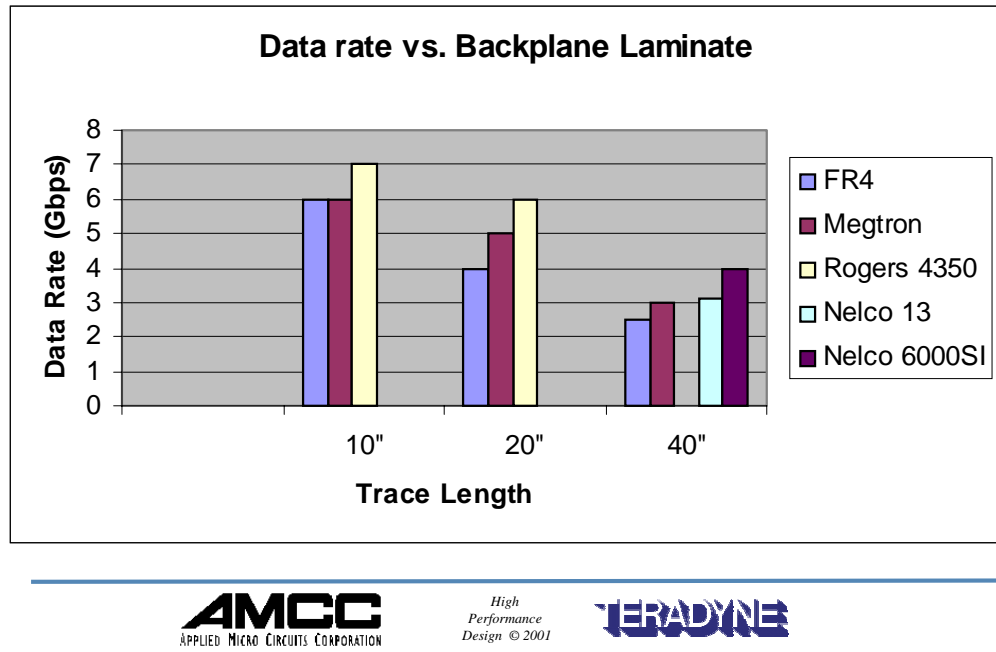


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GbX was analyzed at 10” of Rogers plus 6” of total DC length in FR4 at 4, 5 and 6Gbps. It is obvious that the system performance degrades rapidly from 4Gbps to 6Gbps. The 6Gbps data rate is still passing by the standard of having at least 100mV of eye-opening.



A summary of the data rates that are achievable through various laminates and trace lengths are shown above. The criteria used was that the eye-opening had to be at least 100mV or 20% of the 500mV output voltage swing.

Active Backplane System



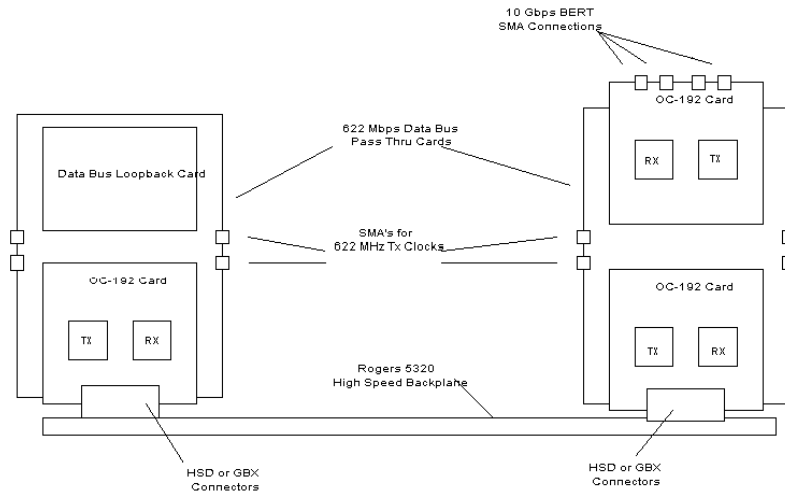
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In this section the Passive Backplane system will be replaced by an active system. The active system consists primarily of an OC-192 serdes chip set and a 622Mhz parallel loop-back board supplied by AMCC.

The Passive system was enhanced by incorporating AMCC's S3091, an OC-192 serializer and S3092, an OC-192 de-serializer that contains a CDR. The CDR along with the serializer/de-serializer will be evaluated for passing these high speed signals.

Diagram of the 10 Gbps Testbed



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First Just One Signal Path:

The 10 Gbps testbed was designed to demonstrate a Bi-Directional Serial Transmission of 10 Gbps Data Streams across backplanes. An intermediate 622 MHz data bus Pass Thru card was used to simulate data bus traffic on a line card.

A 10 Gbps BERT was used to drive the SMA inputs to the Card 1 Rx. This Rx is located on the upper OC-192 card which is connected to the backplane OC-192 card by the 622 MHz data bus Pass Thru card. The backplane OC-192 Card is Card 2 in the signal path. The Tx of card 2 then drives the backplane at 10 Gbps to the OC-192 Card 3 Rx.

The Card3 Rx receives the 10 Gbps serial data and sends it up the 622 Mbps data bus of the Pass Thru card. If a loop back card is installed at the upper OC-192 card location it send the 622 Mbps data back to the card 3 Tx. The Card 3 Tx then send the 10 Gbps serial data back to the card 2 Rx.

The Oc-192 Card 2 Rx then drives the 622 Mbps data bus of the Pass Thru card up to the Upper OC-192 card 1 Tx. And again the card 1 Tx sends the 10 Gbps data back to the BERT and Communications analyzer. The BERT gives data bit error rate information and the Communication Analyzer allows viewing of the Signal Quality and Eye Diagram of the final signal.

Signal Path Options:

Note that there are two types of Card 2 and Card 3's, one set uses HSD connectors and one uses GbX connectors. There are identical paths in the testbed backplane for each connector type. There are also two data path lengths through the backplane, 10" and 20".

Another option is to have another OC-192 type like card 1 to take the card 3 622 MHz output and send it back to the BERT in serial 10 Gbps format after only one pass through the backplane. This would replace the Data Bus Loopback Card.

A third option is to use our original OC-192 loopback card with the Card 3 backplane interface cards in place of the Card 3 Pass Thru loopback combination.

10 Gbps Eval Board Design

- S3091 OC-192 16:1 Mux, Transmitter
 - Silicon Germanium BICMOS Technology
 - OC-192 (9953.28 Mbps)
 - 148-pin CBGA package
- S3092 OC-192 1:16 DeMux, Receiver with CDR and Postamp
 - 148-pin CBGA package



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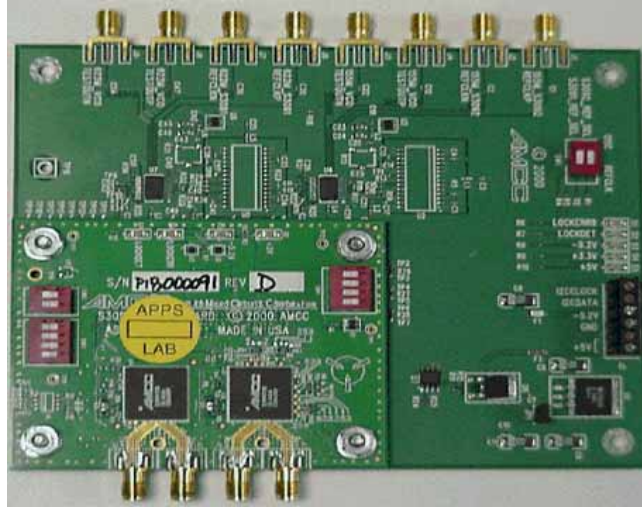


The active system uses AMCC's S3091, an OC-192 serializer as the transmit portion of the link. AMCC's S3092 deserializer was used as the receiver portion of the link. The S3091 serializer takes the 622 Mbps, 16 bit wide differential data bus and serializes the data into a 10Gbps data stream. The output of the S3091 is a Current Mode Logic (CML) driver. This output will drive into the backplane, demonstrating performance through the VHDM-HSD and GbX backplane connectors.

The S3092 deserializer has a 6dB boost amp ahead of its Clock and Data Recovery (CDR) circuits. The CDR will recover clock timing of the incoming data, removing jitter caused by the backplane and connector transitions.

With the recovered timing of the incoming data the lockdet signal will indicate a completed connection with qualified data.

10Gbps Eval Board Test fixture



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This picture shows the combination board set used for the AMCC OC-192 Chipset Evaluation Platform. The smaller board shows the S3091 and S3092 BGA's. The larger board shown under the small board is the 622 MHz data bus Loopback board. The Loopback board also contains SMA connectors to bring in external synchronization clocks and power to both cards. A small power interlock circuit also maintains the correct power up sequencing no matter when the external supplies are powered up.

S3091 OC-192 16:1 Transmitter

- Transmitter Operations:
 - 16 bit parallel input
 - each input is Differential LVDS @ 622MHz
 - Parallel-to-Serial Conversion
 - Serial output using CML technology
 - Typical power 2W



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See your local AMCC rep or visit the AMCC web site at www.AMCC.com for S3091 chip specifics.

S3092 OC-192 1:16 Receiver

- Receiver Operations:
 - Serial input to Limiting Postamp
 - Clock and Data Recovery
 - Serial to Parallel Conversion
 - 16-bit parallel output, Differential LVDS @ 622MHz
 - Typical power 1.6 W



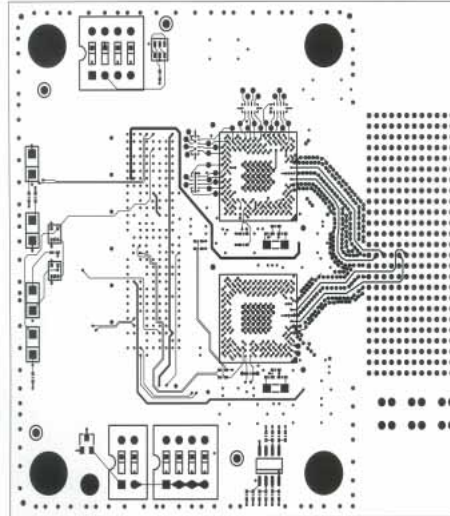
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See your local AMCC rep or visit the AMCC web site at www.AMCC.com for S3092 chip specifics.

OC-192 Card Top Layer

- Top layer is used for the 10 Gbps
- High Speed Traces use Co-Planar Waveguide Structure
- Via's line the Co-Planar Waveguide to maintain the High Frequency components of the signal



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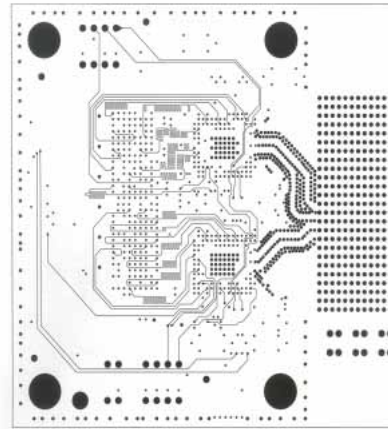
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The specifics of 10 Gbps design are shown in this layout of one of the backplane interface cards. Co-Planar Waveguide structures are used to enter and exit the 10 Gbps ports of the BGA's. These structures are then lined with via's to assist in maintaining the edge speeds of the signals. These edge speeds are on the order of 25 to 35 ps rise and fall times.

The top layer of this PCB is made up of RO-4003 material. This material is easy to work with in a hybrid stackup of GETEK or HT-FR4.

OC-192 Card Inner Signal Layer

- Signal Layer 4 showing serpentine traces
- Matched Length Data bus lines are required at 622 Mbps Data Rates
- Tolerance on Matching depends on Total System Trace Length
- For this PCB Data bus lines were matched to 0.050" or ~8ps



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Inner traces for the 622 Mbps data bus are shown in this diagram. Matched length considerations are highlighted in the bullets.

The key to matched length design is to come up with an allowable system skew budget. Then to distribute those budget pieces over the cards affected. Manufacturing tolerances or board layout considerations will all come into the picture. Connector and via effects must also be taken into account. Board materials for these layers may be different than the top High Speed layer. One method I have used with good success is making a spreadsheet with all the effects represented and totaled at the bottom. This allows most of the effects of a high speed design to be consistently taken into account.

OC-192 PCB Stackup

Filename: Stackup_S3091-3092-HSD_1oz.xls
 Updated: 1/27/01
HSD Board Stackup **1oz Copper Pre-Fab Stackup**

Layer #	Layer Type	Dielectric Thickness mils	Cu Thickness mils	Material	Thermal Conductivity	Cu_oz	Er	Trace Width, mils	Controlled Impedance
	Conformal Coat								
1	Signal/GND		2.1	Cu		1/2 (1 1/2)		17W GCPW 9G	50
	Dielectric	8		RO-4003	0.2		3.38		
2	GND		0.7	Cu		1/2			GND1
	Dielectric	3		GETEK			3.8		
3	Pwr1_-5.2V		1.4	Cu		1			-5.2V PWR
	Dielectric	7		GETEK			3.8		
4	Signal/GND		1.4	Cu		1		4	
	Dielectric	5		GETEK			3.8		100
5	Signal/GND		1.4	Cu		1		4	
	Dielectric	7		GETEK			3.8		
6	Pwr1_+3.3V		1.4	Cu		1			+3.3V PWR
	Dielectric	3		GETEK			3.8		
7	GND		1.4	Cu		1			GND
	Dielectric	7		GETEK			3.8		
8	Signal/GND		1.4	Cu		1		4	
	Dielectric	5		GETEK			3.8		100
9	Signal/GND		1.4	Cu		1		4	
	Dielectric	7		GETEK			3.8		
10	GND/Signal		2.1	Cu		1/4 (1 1/2)		tbd	GND
	Conformal Coat								
Totals		52	14.7 = 66.7 mils			(Plated Up)			
Total Board Thickness		0.063 +- 0.006 mils							
Top layer plated up to 1 1/2 oz thickness, bottom layer plated as necessary									
Controlled Impedance on layer 1 of 50 ohm Co-Planar transmission line, +- 4 ohms									
Controlled Differential Impedance on layers 4&5 and 8&9 of 100 ohms line to line +-4 ohms Broadside Coupled Stripline									
Board Dimensions: -3.75" x 3.5"									



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This OC-192 PCB stackup spread sheet is a very useful tool to use as you put together a High Speed PCB Design. Features are Layer by Layer Stackup info, Dielectric and copper thickness, material type, thermal conductivity, tracewidth and controlled impedance notes. PCB stackup thickness is totaled at the bottom.

Fabrication notes are also maintained for mechanical and electrical performance spec's.

Board Testing Stages

- Single Board Testing with VHDM-HSD and GbX backplane connector boards with SMA connections
 - Allows loopback testing of the Receiver thru the Transmitter at 10 Gbps with the BERT
 - Verified both the 10 Gbps data path and the 622 Mbps data bus paths
 - Allows visibility of 10 Gbps Signal Integrity



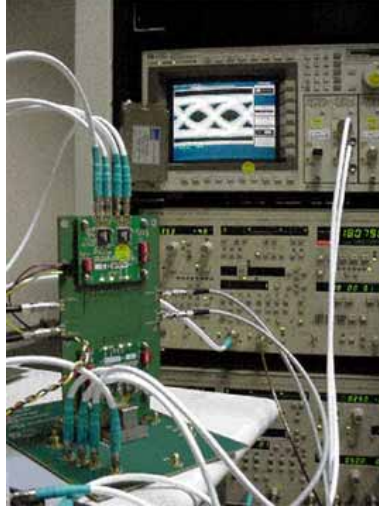
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OC-192 board testing involves checkout of each functional signal path. If these signal paths can be verified individually you will build a system on a solid foundation and save yourself a lot of checkout time at the system level.

This can be accomplished by checking out each OC-192 card individually before they are integrated into the system testbed.

Dual Tx-Rx Board with backplane connector test fixture



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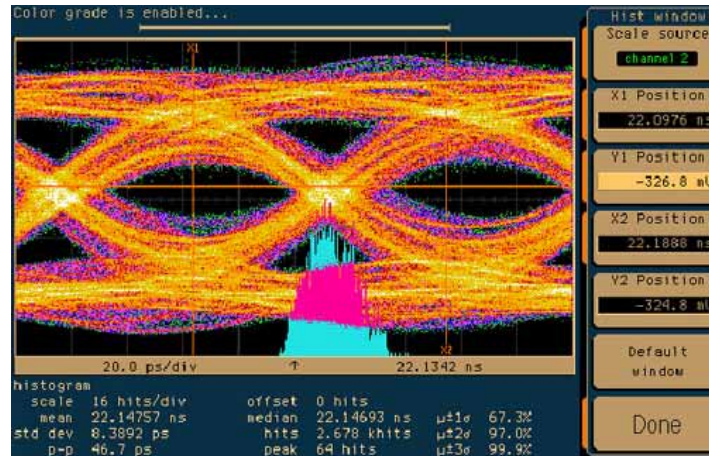
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After testing the OC-192 cards individually you are ready to integrate them into a 622 Mbps Pass Thru card assembly. This picture shows that assembly being tested with the backplane connector test card.

10 Gbps Eye Diagram

- Output from final OC-192 Tx through one VHDM-HSD 8 row connector



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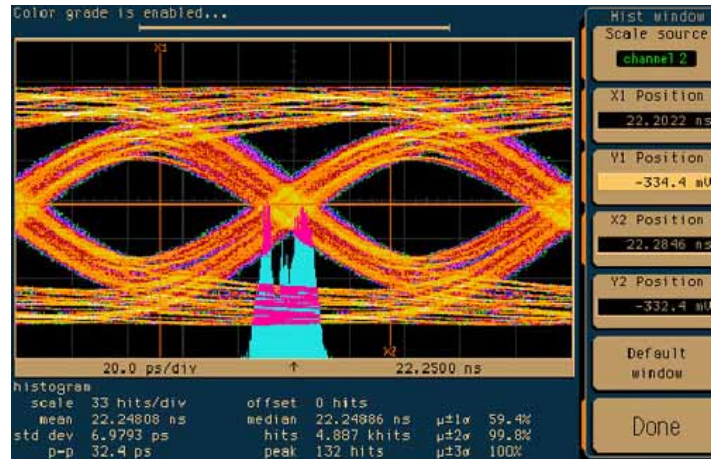
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This eye diagram shows the output from the backplane test fixture and the OC-192 card with an HSD connector. Note the backplane test fixture PCB has 6" of traces in FR4 material.

10 Gbps Eye Diagram

- Output from final OC-192 Tx through one GbX 8 row Connector



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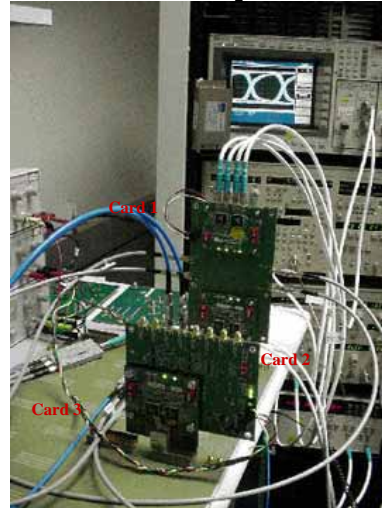
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This eye diagram shows the output of a similar backplane test fixture and the OC-192 card with a GbX connector.

Complete Testbed Setup

- Bert driving 10 Gbps serial into Card 1
- Card 1 driving Card 2 then into backplane at 10 Gbps
- Card 3 Receiving 10 Gbps and Looping back to Card 2
- Card 2 Receiving 10 Gbps and driving Card 1 then 10 Gbps back to the BERT



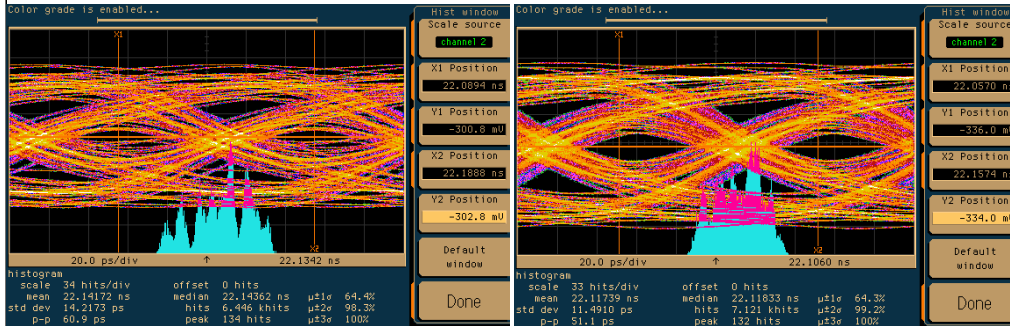
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Our first cut at the complete testbed running together is shown in this slide. Follow the slide bullets for the signal path. Note that each time the 10 Gbps signal transitions into an S3092 Rx, the CDR will clean up the jitter. Therefore the final jitter out of the last OC-192 card into the BERT will mostly have the jitter associated with the final trace paths of the last OC-192 Tx and the cables to the BERT. Therefore if you look at the eye diagram on the communications analyzer you will see a very nice OC-192 eye with ~20 ps of jitter.

GbX over 10" of Rogers



Driven By BERT
plus 6" of FR4

Driven by OC-192 Transmitter
plus 3" FR4 and 3" of RO4003

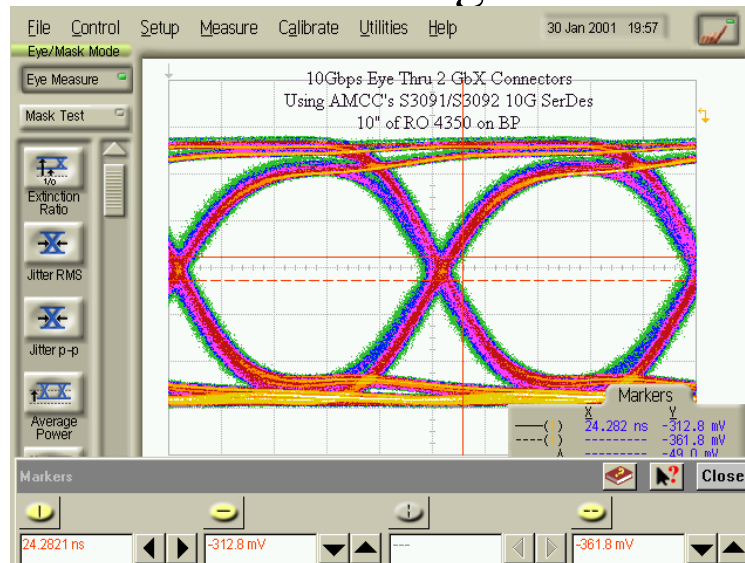


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These eye diagrams show the difference between a BERT driving a 10" Rogers backplane with GbX connectors and the S3091 Tx driving the same backplane. The only difference is the BERT is driving its cables and 3" more of FR4.

GbX over 10" of Rogers w/SerDes



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This Eye-Diagram shows a 10Gbps data rate being passed through 2 GbX connectors and 10 inches of a Rogers 4350 backplane. In addition a set of AMCC S3091/S3092 10Gbps Serdes chipset was used on both GbX daughter cards. A detailed description of the S3091/92 chipset and the GbX connector can be found in previous slides. It is clear that with the aid of the AMCC SerDes and using a high performance connector such as GbX and high performance materials(Rogers 4350) that 10Gbps data rates can be achieved in a backplane environment. The backplane **did not** incorporate any of the techniques previously described in reducing the capacitive effect of the Plated Through Hole such as counter-boring, dual density drilling, or minimizing the stub effect. The only feature used was the non-circular anti-pad around the signal pairs.