
EE273 Lecture 1

Introduction to Digital Systems Engineering

January 10, 2001

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Today's Lecture

- Logistics
- What is *Digital Systems Engineering*
- Transmission Line Basics

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Logistics

- See the course policy sheet for details
 - Lectures: MW 11:00 to 12:15 in Skillings Aud.
 - Textbook: Dally and Poulton, *Digital Systems Engineering*
 - Grading
 - 20% weekly problem sets
 - 20% class project
 - 25% midterm exam (2/12 in the evening)
 - 35% final exam
 - Collaboration encouraged on problem sets and project groups of up to 3 people
 - single solution
 - all assistance acknowledged
 - SITN Local and Stanford on-line only (no TVI)
 - no delay

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More Logistics

Course Staff	Instructor	Bill Dally
	TAs	Patrick Chiang Greg Larchev
	Support	Pamela Elliott
Late Policy	problem sets due at the beginning of class one week from the date of assignment no credit for late assignments SITN/Stanford on-line assignments and exams due at the same time	

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Yet More Logistics

Exams	Midterm	February 12 7PM-9PM We will still have class that day Local SITN students must come to campus
	Final	March 23 8:30 to 10:30
Assignments	assigned each Wednesday due at beginning of class the following Wednesday	
Reading	assigned for each class. Complete reading before the corresponding class	
Graders	submit application if interested full credit on homework and \$\$\$	

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Today's Assignment

-
- Reading
 - Chapter 1
 - Sections 3.1 through 3.3
 - Complete before next Wednesday 1/17
 - Problem Set 1
 - Problems 3-2 and 3-10
 - Due at the start of class on Wednesday 1/17

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What is Digital Systems Engineering

- System level electrical design
 - noise management
 - keeping signals clean
 - signaling
 - moving bits from here to there
 - timing
 - how we know when a new bit is here
 - power distribution
 - DC voltage with AC current



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Why is Digital Systems Engineering Important?

- System-level electrical issues are becoming more critical
 - Higher clock rates
 - wires are transmission lines
 - clock skew and jitter are a major portion of a clock cycle
 - many cables are more than one clock long
 - Lower voltages
 - more current for a given power level
 - less margin
 - Pin bottlenecks
 - need to make each signal count
- Its not just for supercomputers anymore
- Get it right or it doesn't work
- 'Cookbook' approaches aren't adequate - need analysis

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This Course Will Teach You

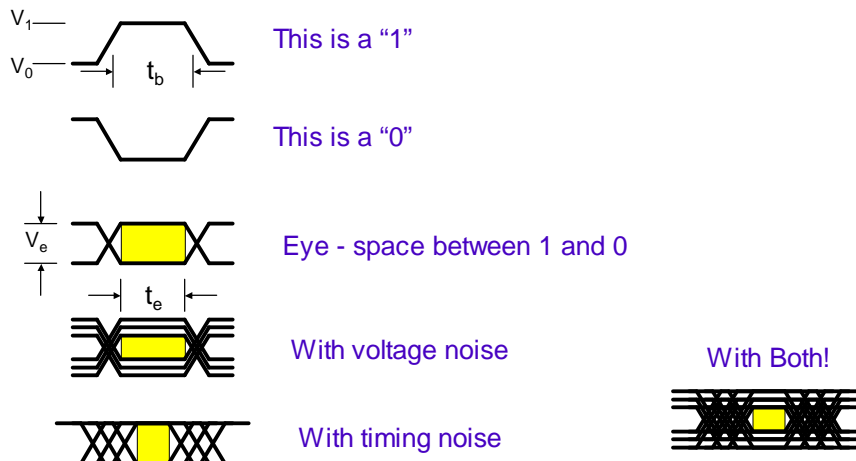
- To *understand* system-level electrical issues
 - understand the phenomena
 - develop engineering models for simulation and analysis
 - develop and evaluate solutions
- To design systems that work reliably the first time
 - noise budgets
 - timing budgets
- To push performance where its needed
 - signaling rates
 - synchronization latency and failure probability
 - power distribution

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The Eye Diagram A View of Noise, Signaling, and Timing



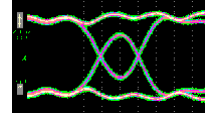
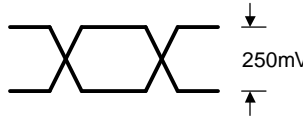
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An Example Noise Calculation

- 250mV differential signal
- 15% high-frequency attenuation
- 5% crosstalk from adjacent lines
- 5% ISI from reflections
- 20mV receiver offset+sensitivity
- 10mV RMS Gaussian noise
- What is the Bit Error Rate?



Signal Swing (dp-dn)		500
Gross Margin		250
Crosstalk	0.05	25
Reflections	0.05	25
Attenuation	0.15	75
KN	0.25	125
Receiver offset+sensitivity		20
Bounded noise		145
Net Margin		105
Gaussian Noise		10
VSNR		10.5
BER		1.15E-24

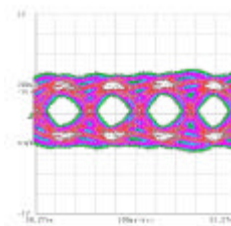
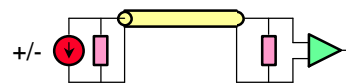
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Signaling

- How to move a symbol (usually a bit) from here to there
 - how is the symbol represented?
 - "0" = -2.5mA, "1" = 2.5mA
 - how is the line terminated at each end?
 - Z_0 at both ends
 - how are references generated?
 - Differential signal
 - how does the receiver detect the symbol?
 - detect voltage across terminator



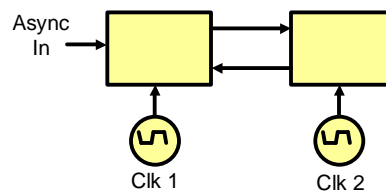
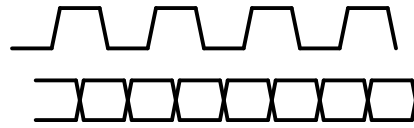
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Timing and Synchronization

- How do you determine when a symbol is valid? (when a new symbol arrives?)
- Synchronous timing
 - all FFs driven by one clock
 - may be 10^5 FFs/chip 10^7 in a system
 - wires may be > 1 clock long
 - skew is a **big** problem
- Pipeline timing
- Self-timed design
- Multiple clock domains
 - signals must be synchronized



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Power Distribution

- Consider a system with
 - 100 20A chips (2KA)
 - A 400MHz clock ($t_{ck} = 2.5ns$)
 - Current can drop to zero in one clock cycle
 - $di/dt = 2KA/2.5ns = \underline{\hspace{2cm}}$
- What does a 1nH inductor in series with this supply current do?
- How do we solve this problem?

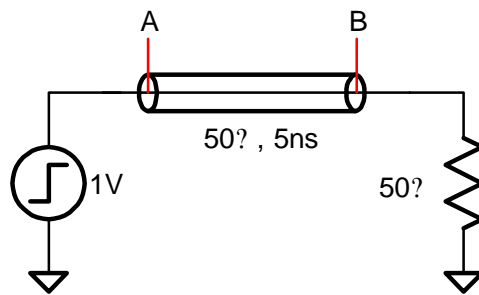
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Wires are Transmission Lines

- Three basic rules of transmission lines
 - Waves propagate down the line (in both directions)
 - Waves reflect unless terminated
 - The voltage is the **superposition** of these waves



What is the response at point B on this line to a unit step at point A?

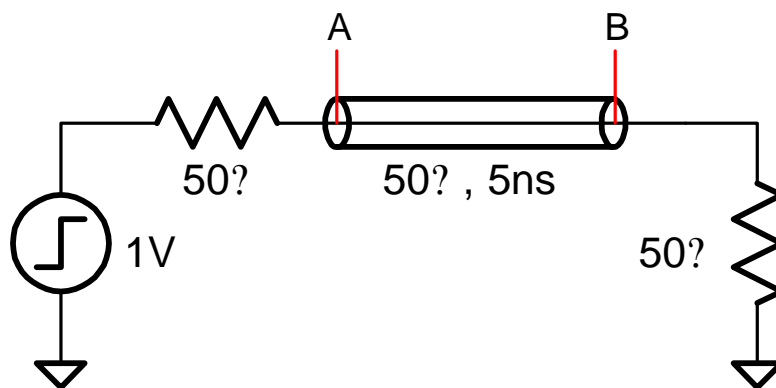
What if the waveform on A is changed?

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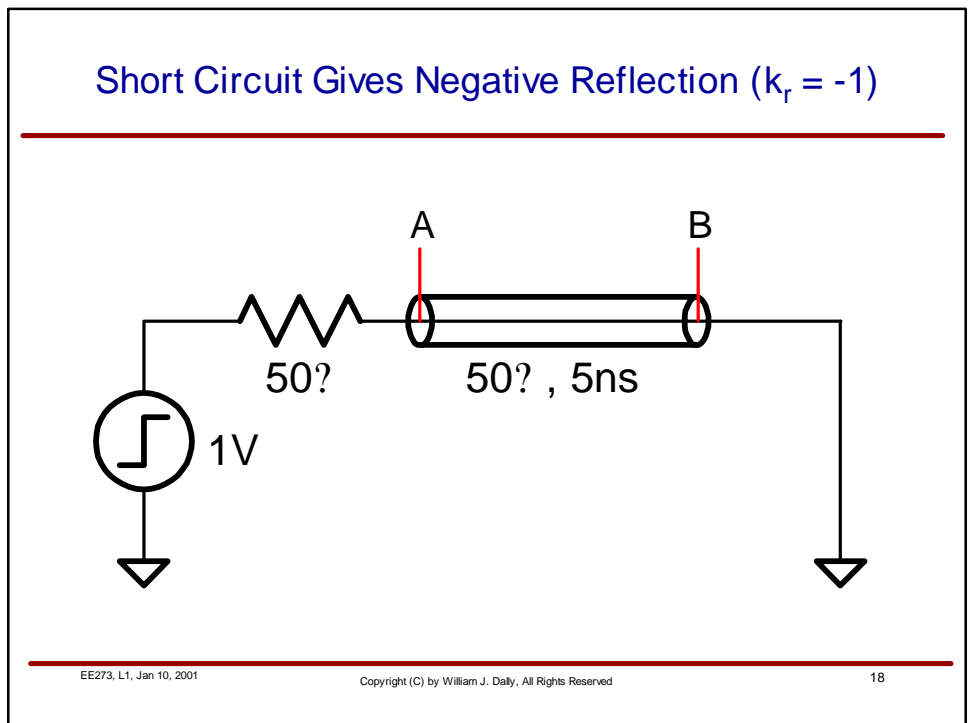
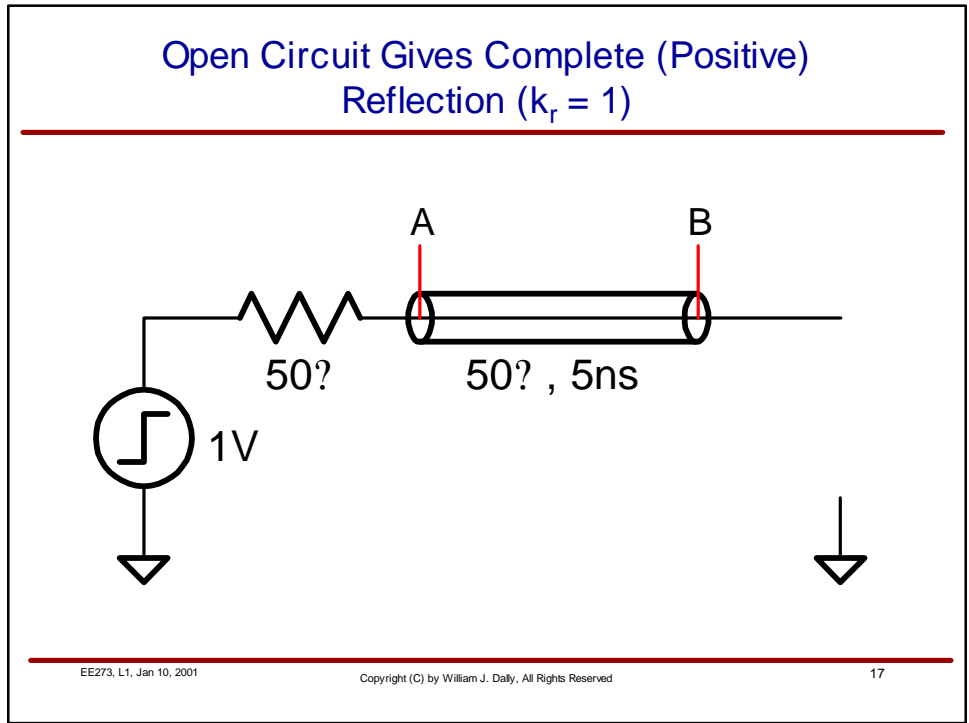
Waves Reflect From Improper Terminations



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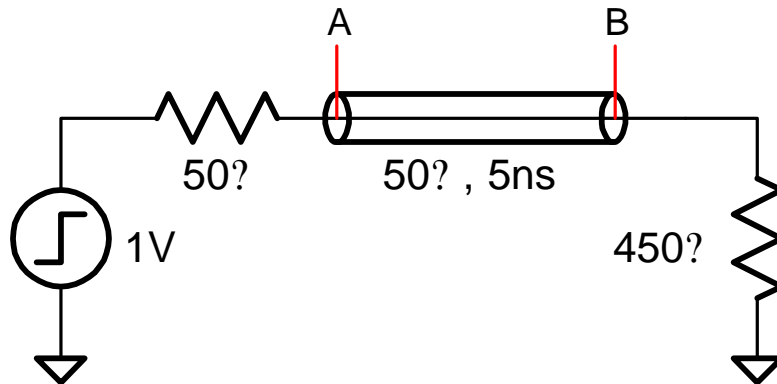
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In general, reflection coefficient is determined by the Telegrapher's Equation

$$k_r = \frac{Z_T - Z_0}{Z_T + Z_0} = \frac{450 - 50}{450 + 50} = 0.8$$

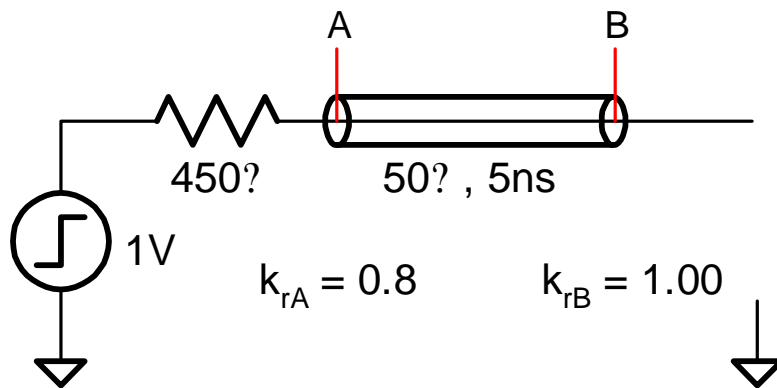


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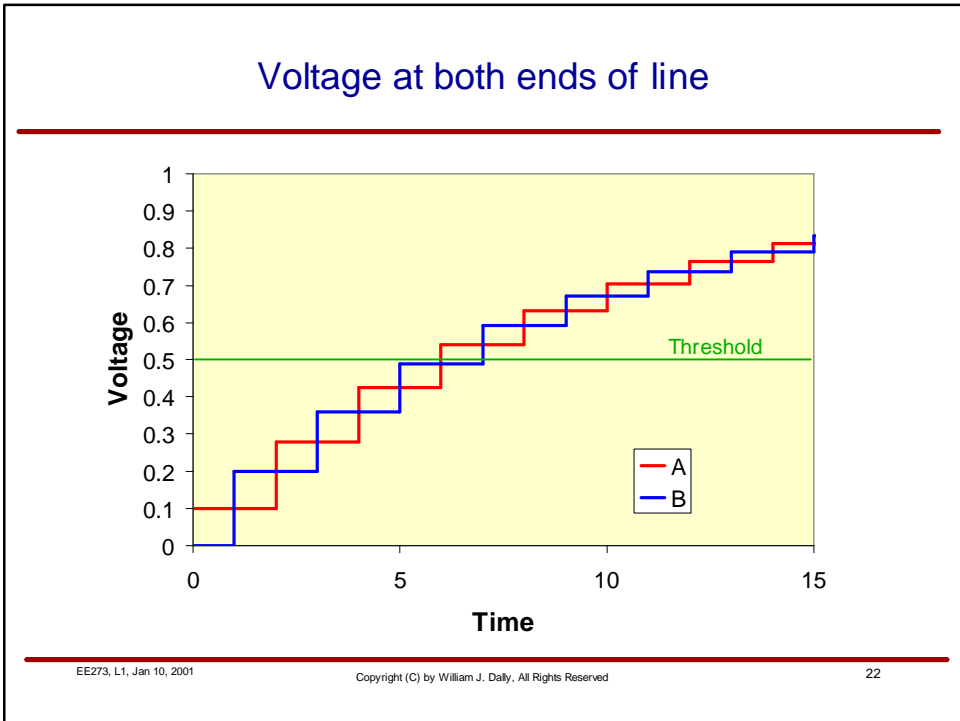
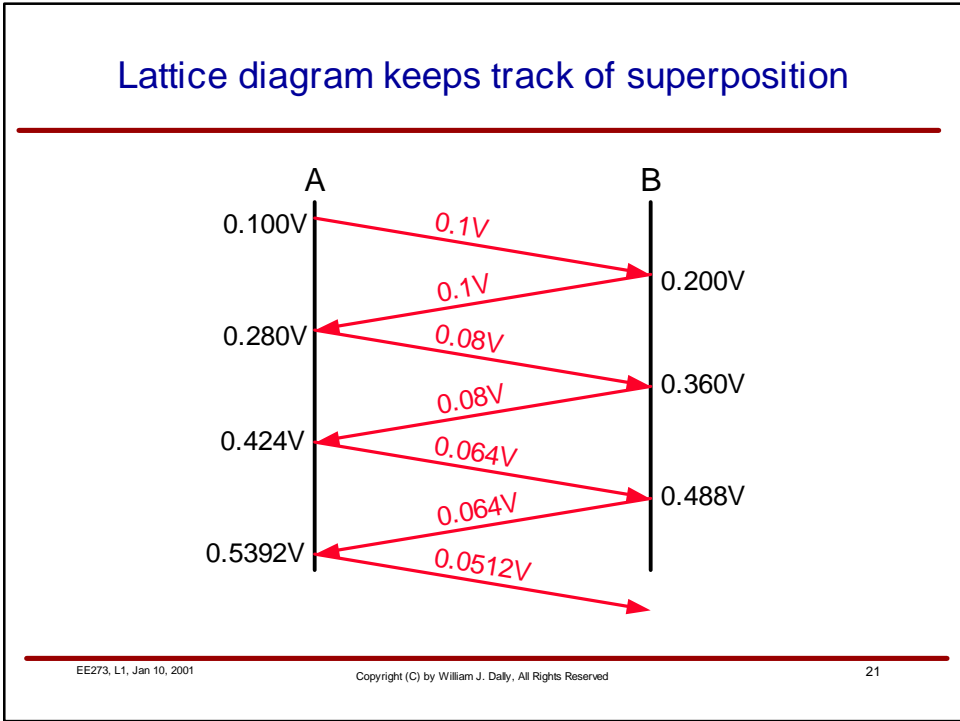
Reflections Happen from **Both** ends

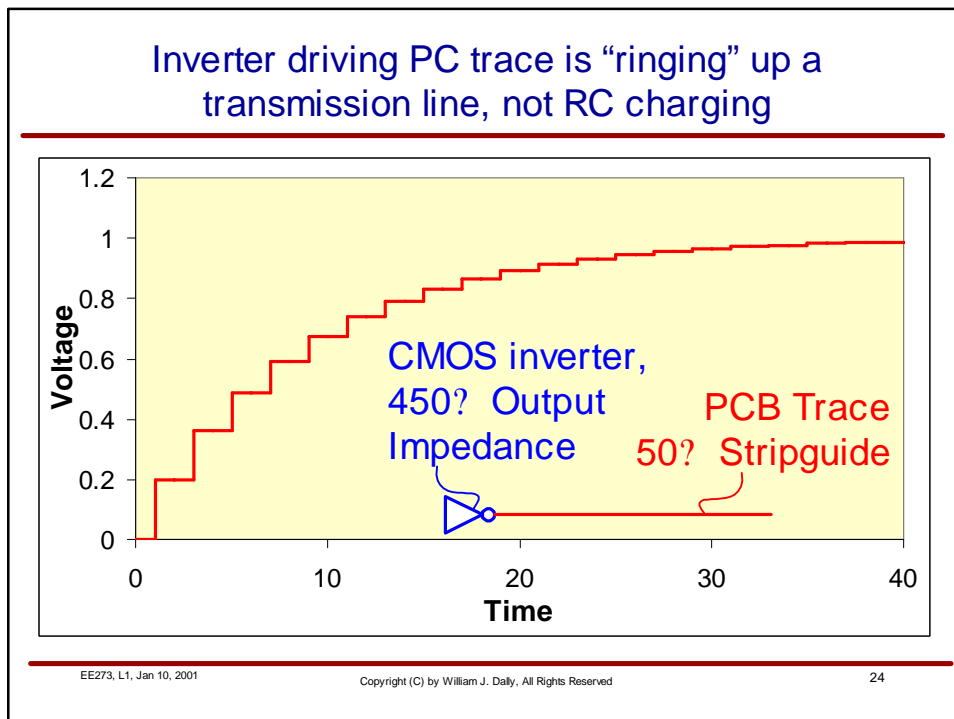
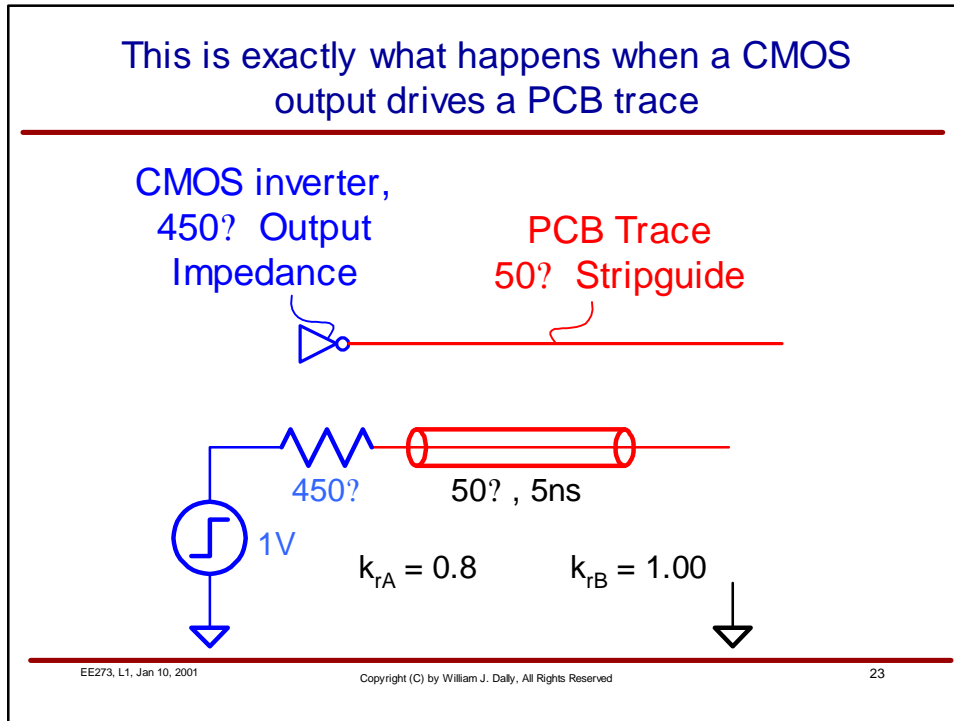


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Next Time

- Introduction to wires
 - electrical properties of wires
 - simple transmission lines
 - terminations and reflections
 - lossy transmission lines