Today's Lecture

- Logistics
- What is Digital Systems Engineering
- Transmission Line Basics
Logistics

• See the course policy sheet for details
  Lectures:  MW 11:00 to 12:15 in Skillings Aud.
  Textbook:  Dally and Poulton, *Digital Systems Engineering*
  Grading:  20% weekly problem sets
            20% class project
            25% midterm exam (2/12 in the evening)
            35% final exam
  Collaboration: encourged on problem sets and project
                 groups of up to 3 people
                 single solution
                 all assistance acknowledged
  SITN:  Local and Stanford on-line only (no TVI)
         no delay

More Logistics

Course Staff:  Instructor:  Bill Dally
               TAs:  Patrick Chiang, Greg Larchev
               Support:  Pamela Elliott

Late Policy:  problem sets due at the *beginning* of class one
              week from the date of assignment
              *no* credit for late assignments
              SITN/Stanford on-line assignments and exams
              due at the same time
Yet More Logistics

Exams
- Midterm: February 12 7PM-9PM
  - We will still have class that day
  - Local SITN students must come to campus
- Final: March 23 8:30 to 10:30

Assignments
- assigned each Wednesday
  - due at **beginning** of class the following Wednesday

Reading
- assigned for each class. Complete reading **before** the corresponding class

Graders
- submit application if interested
  - full credit on homework and $$$

Today’s Assignment

- **Reading**
  - Chapter 1
  - Sections 3.1 through 3.3
  - Complete before next Wednesday 1/17

- **Problem Set 1**
  - Problems 3-2 and 3-10
  - Due at the start of class on Wednesday 1/17
What is Digital Systems Engineering

- System level electrical design
  - noise management
    - keeping signals clean
  - signaling
    - moving bits from here to there
  - timing
    - how we know when a new bit is here
  - power distribution
    - DC voltage with AC current

Why is Digital Systems Engineering Important?

- System-level electrical issues are becoming more critical
  - Higher clock rates
    - wires are transmission lines
    - clock skew and jitter are a major portion of a clock cycle
    - many cables are more than one clock long
  - Lower voltages
    - more current for a given power level
    - less margin
  - Pin bottlenecks
    - need to make each signal count
- Its not just for supercomputers anymore
- Get it right or it doesn't work
- ‘Cookbook’ approaches aren’t adequate - need analysis
This Course Will Teach You

• To understand system-level electrical issues
  – understand the phenomena
  – develop engineering models for simulation and analysis
  – develop and evaluate solutions
• To design systems that work reliably the first time
  – noise budgets
  – timing budgets
• To push performance where it is needed
  – signaling rates
  – synchronization latency and failure probability
  – power distribution

The Eye Diagram
A View of Noise, Signaling, and Timing

This is a “1”

This is a “0”

Eye - space between 1 and 0

With voltage noise

With timing noise

With Both!
An Example Noise Calculation

- 250mV differential signal
- 15% high-frequency attenuation
- 5% crosstalk from adjacent lines
- 5% ISI from reflections
- 20mV receiver offset+sensitivity
- 10mV RMS Gaussian noise
- What is the Bit Error Rate?

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<table>
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<tbody>
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Signaling

- How to move a symbol (usually a bit) from here to there
  - how is the symbol represented?
    - “0” = -2.5mA, “1” = 2.5mA
  - how is the line terminated at each end?
    - $Z_0$ at both ends
  - how are references generated?
    - Differential signal
  - how does the receiver detect the symbol?
    - detect voltage across terminator
Timing and Synchronization

• How do you determine when a symbol is valid? (when a new symbol arrives?)
• Synchronous timing
  – all FFs driven by one clock
  – may be $10^8$ FFs/chip $10^7$ in a system
  – wires may be $>1$ clock long
  – skew is a big problem
• Pipeline timing
• Self-timed design
• Multiple clock domains
  – signals must be synchronized

Power Distribution

• Consider a system with
  – 100 20A chips (2KA)
  – A 400MHz clock ($t_{ck} = 2.5$ns)
  – Current can drop to zero in one clock cycle
  – $\frac{di}{dt} = \frac{2KA}{2.5ns} = \ldots$
• What does a 1nH inductor in series with this supply current do?
• How do we solve this problem?
Wires are Transmission Lines

- Three basic rules of transmission lines
  - Waves propagate down the line (in both directions)
  - Waves reflect unless terminated
  - The voltage is the superposition of these waves

What is the response at point B on this line to a unit step at point A?

What if the waveform on A is changed?
Open Circuit Gives Complete (Positive)
Reflection ($k_r = 1$)

Short Circuit Gives Negative Reflection ($k_r = -1$)
In general, reflection coefficient is determined by the Telegrapher’s Equation

\[ k_r = \frac{Z_T - Z_0}{Z_T + Z_0} = \frac{450 - 50}{450 + 50} = 0.8 \]

Reflections Happen from Both ends

\[ k_{rA} = 0.8 \quad k_{rB} = 1.00 \]
Lattice diagram keeps track of superposition

Voltage at both ends of line
This is exactly what happens when a CMOS output drives a PCB trace

CMOS inverter, 450? Output Impedance

PCB Trace 50? Stripguide

\[ k_A = 0.8 \quad k_B = 1.00 \]

Inverter driving PC trace is “ringing” up a transmission line, not RC charging

\[ k_A = 0.8 \quad k_B = 1.00 \]
Next Time

- Introduction to wires
  - electrical properties of wires
  - simple transmission lines
  - terminations and reflections
  - lossy transmission lines