
EE273 Lecture 3

Wires Concluded

Multidrop Buses, Balanced Lines, and Measurement Techniques

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William J. Dally
Computer Systems Laboratory
Stanford University
billd@csl.stanford.edu

Announcement

- Transmission line and crosstalk demo will be held during problem session on 2/9/01.

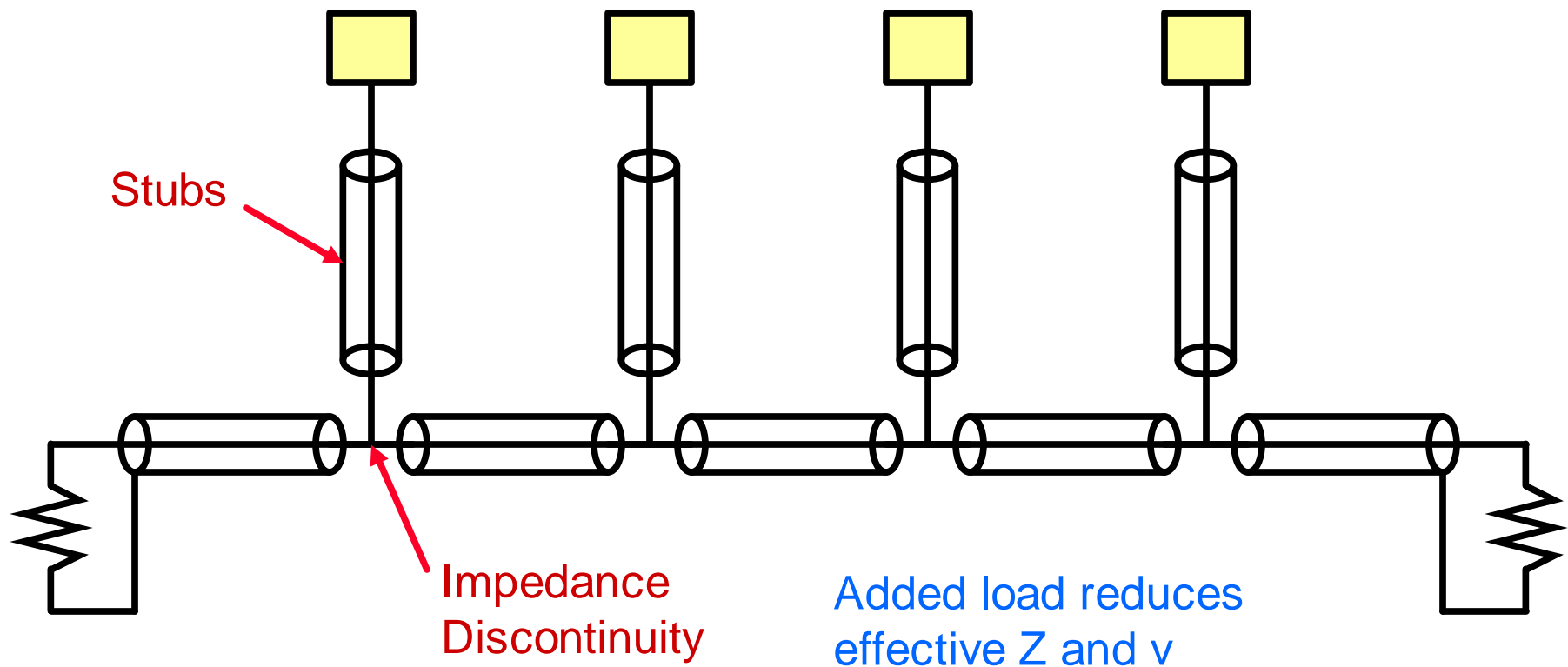
Today's Assignment

- Reading
 - Sections 6.1 through 6.3
 - Complete before class on Wednesday 1/24/00

A Quick Overview

- Multi-Drop Buses
 - stubs and discontinuities
 - frequency limitations
- Balanced lines
 - common and differential mode excitation
 - odd and even mode impedance
 - rise on signal is accompanied by fall on return
- Modeling wires
 - build a model to capture relevant electrical properties
 - ignore inessential elements
 - depends on rise time
- Time-Domain Reflectometer
 - oscilloscope plus pulse generator
 - how to interpret the results

Multi-drop Buses

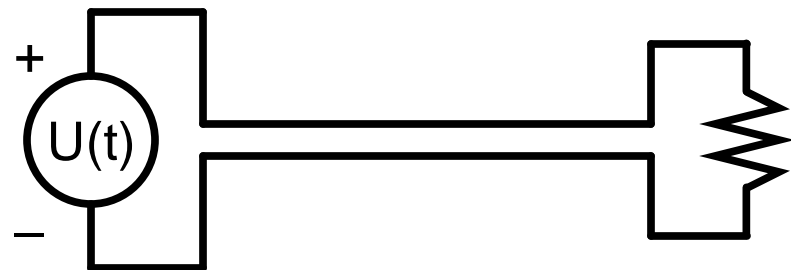
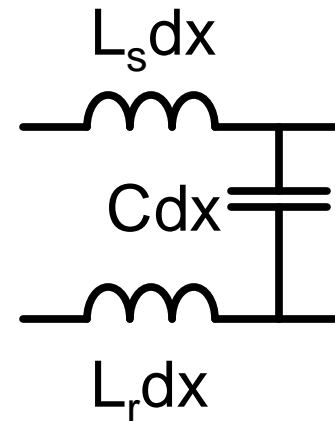


Multi-Drop Buses

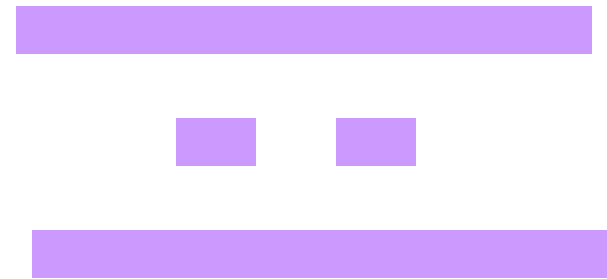
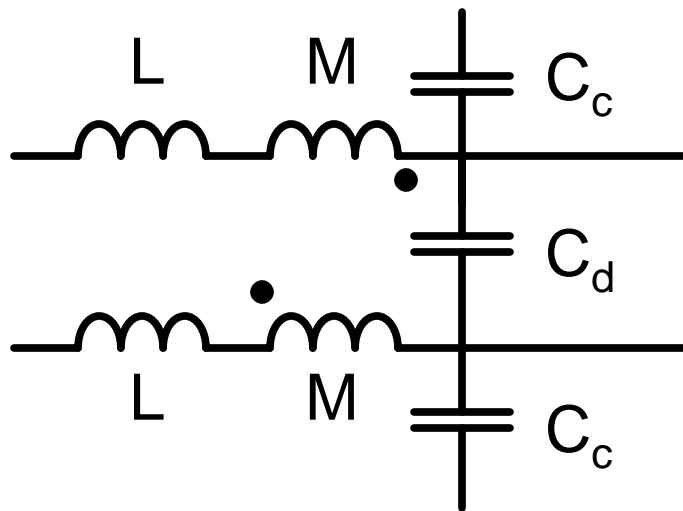
- Consider a typical bus
 - 50 Ω PC board traces
 - C = 100pF/m, L=300nH/m
 - Stubs are 10cm long (0.7ns)
 - 20pF load at end
 - Spacing between modules is 3cm
- Constraints:
 - rise time must be *long* compared to stub length (>3ns) and spacing (>1ns)
 - 30pF each 3cm brings C to 1100pF/m
 - Z = 16.5 Ω , v=5.5 x 10⁷ m/s
 - driver sees 8.25 Ω
- Bus speed is limited by geometry of the bus
 - stub length
 - stub spacing
- Leaving a module ‘unplugged’ causes a discontinuity
- Point-to-point signaling
 - is electrically much cleaner
 - allows concurrent transfers
- ‘Just say no’ to buses
- If you must use a bus, ‘fold’ the stubs

Balanced Transmission Lines

- All transmission lines have inductance in the return path
 - leads to a shift in return voltage across line
- In a balanced line, return inductance equals signal inductance
- Suppose we put a 1V step into a balanced line
 - 0.5V drop across signal inductor
 - 0.5V drop across return inductor
- Remember, we can only name one point GND



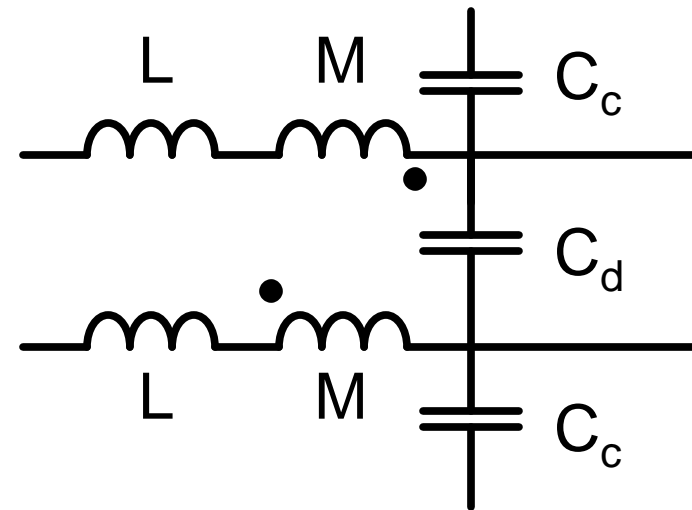
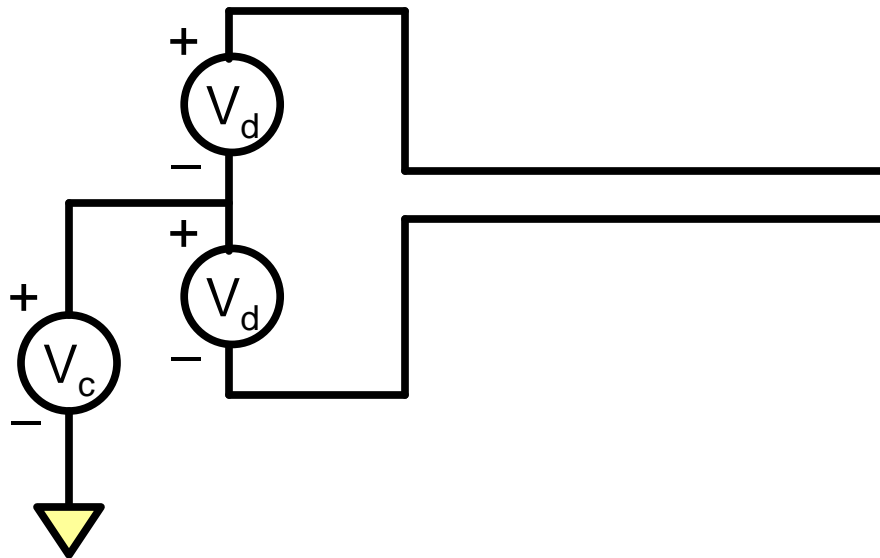
Even and Odd Mode Impedance



e.g., pair of strip guides
between ground planes

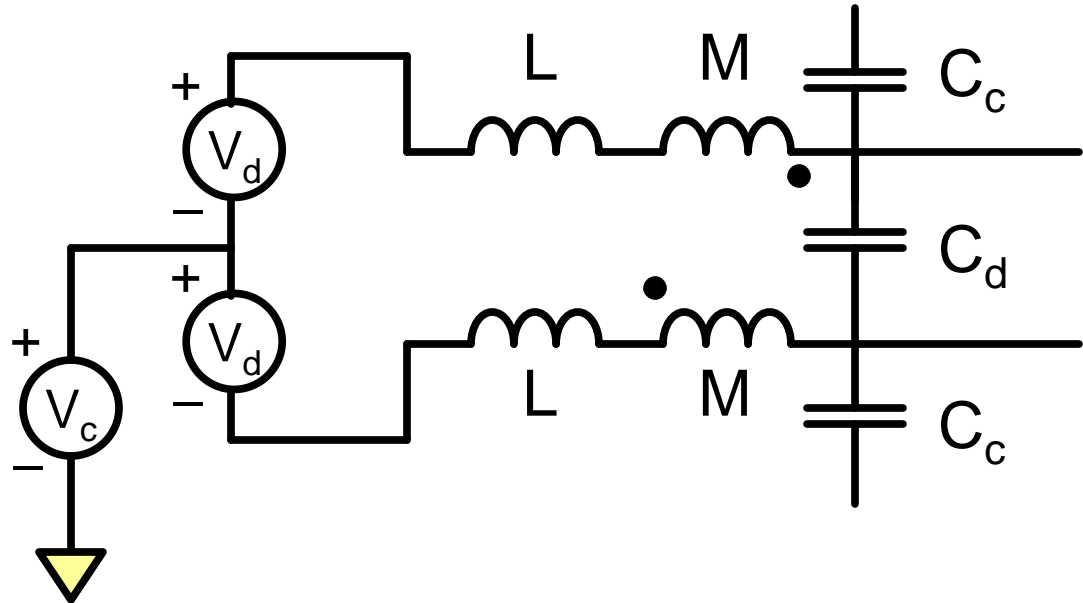
- M and C_d represent coupling between lines
- L and C_c represent coupling to other conductors

Common and Differential Mode Excitation



- Any excitation can be described as the superposition of a *differential* signal and a *common-mode* signal
 - e.g. 1V step: $V_c = 0.5V$, $V_d = 0.5V$

Even and Odd Mode Impedance



$$Z_O = \frac{V_D}{I_1} = \left(\frac{L - M}{C + C_D} \right)^{1/2}$$

$$Z_E = \frac{V_C}{I_1} = \left(\frac{L + M}{C - C_D} \right)^{1/2}$$

$$C = C_C + C_D$$

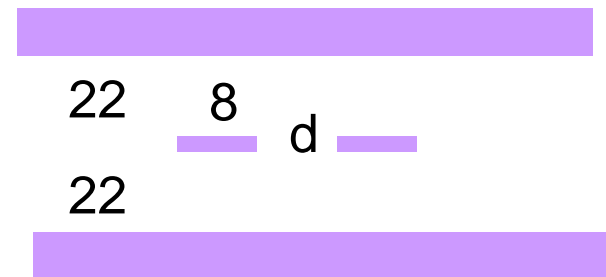
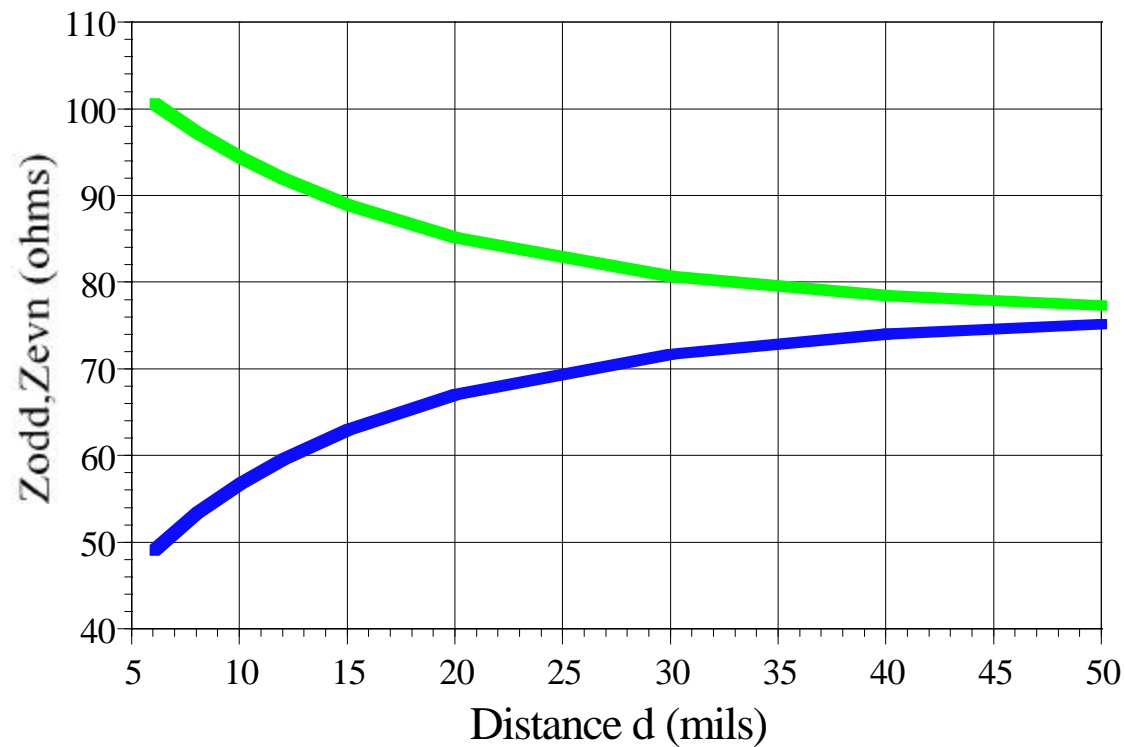
$$\frac{L}{M} = \frac{C}{C_D}$$

- Common and differential-mode signals see different impedance

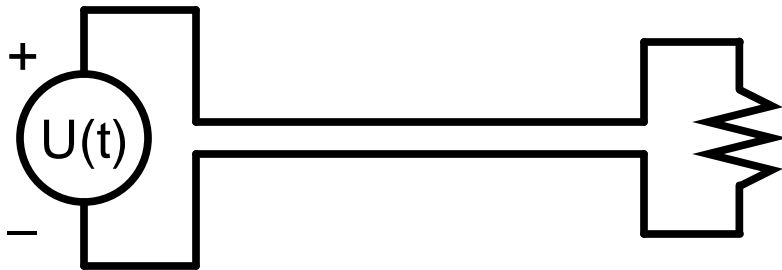
Definitions

- Even-mode impedance, Z_E
 - impedance seen on each line by a common-mode signal
- Odd-mode impedance, Z_O
 - impedance seen on each line by differential mode signal
- Differential impedance, $Z_D = 2Z_O$
 - impedance seen across a pair of lines by differential mode signal
- Common-mode impedance, $Z_C = 0.5Z_E$
 - impedance seen between a pair of lines and a common return by a common-mode signal.

Example of Even and Odd mode impedances

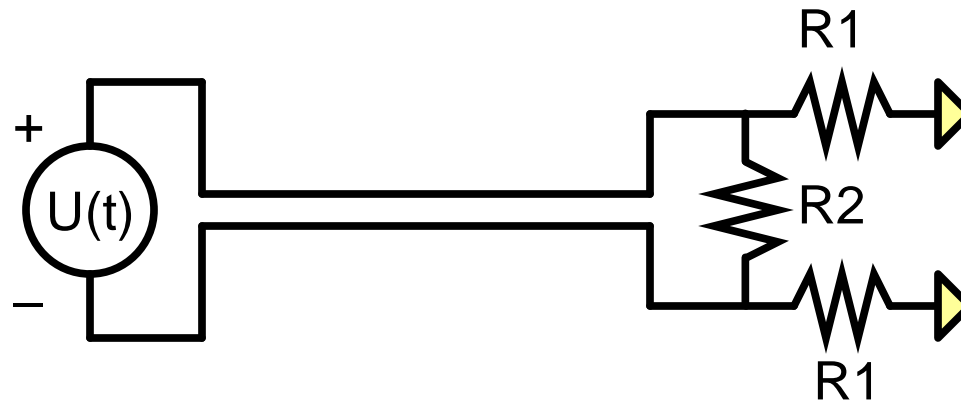


Terminating Even and Odd Modes



- Suppose $Z_O=50\Omega$ and $Z_E=100\Omega$.
- What happens to a 1V step on the line above?
- How should the line be terminated?
- Mode coupling

Terminating Even and Odd Modes



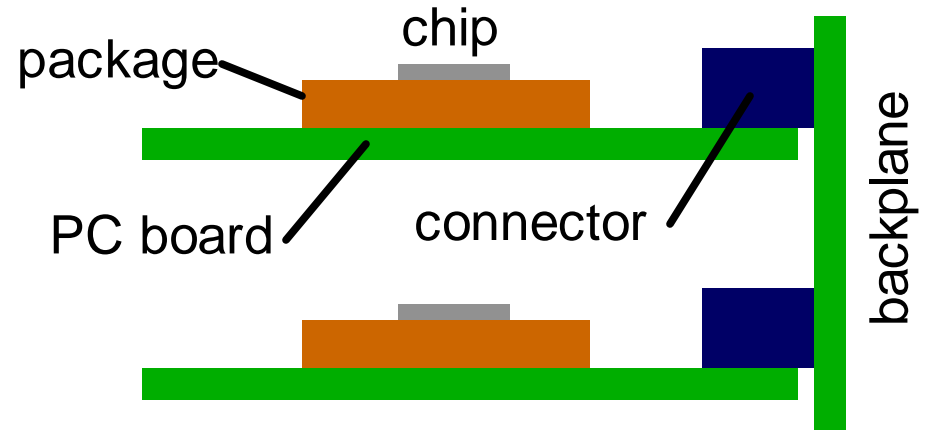
$$R1 = Z_E$$

$$R2 = 2 \left(\frac{Z_E Z_O}{Z_E - Z_O} \right)$$

$$Z_O = R1 \parallel R2$$

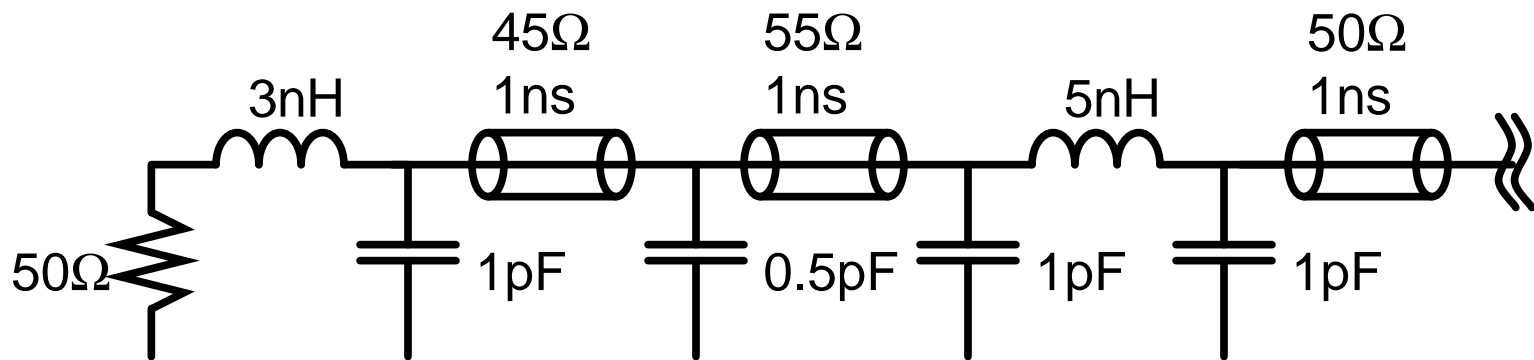
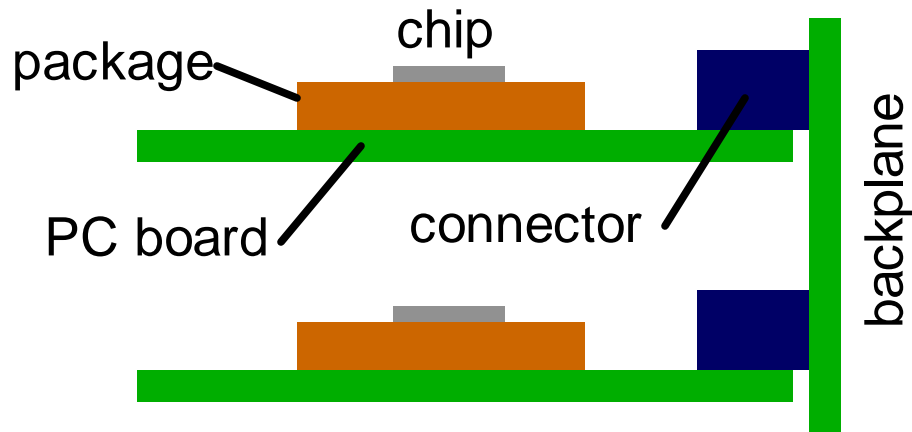
Modeling of Wires

- Given a real system
 - chips, packages, boards, connectors, backplanes, cables
- Need to develop a *model* of the signaling medium
 - for hand calculation of key properties
 - for SPICE simulations
- Model must
 - capture all *relevant* wire properties
 - transmission line properties
 - *major* discontinuities
 - terminations
 - ignore those that are not relevant
 - e.g., short discontinuities



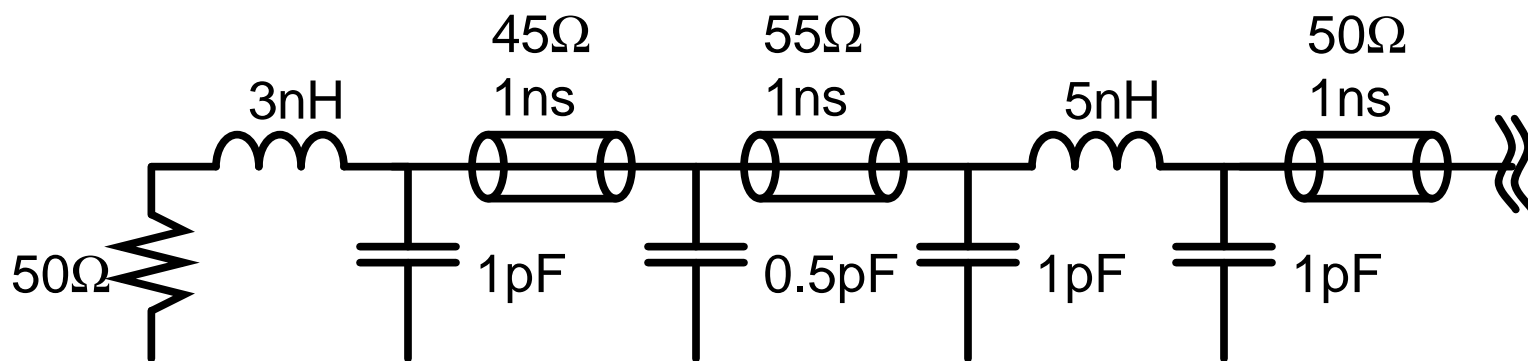
- A good model captures the *relevant* behavior while being as simple as possible

Example Model



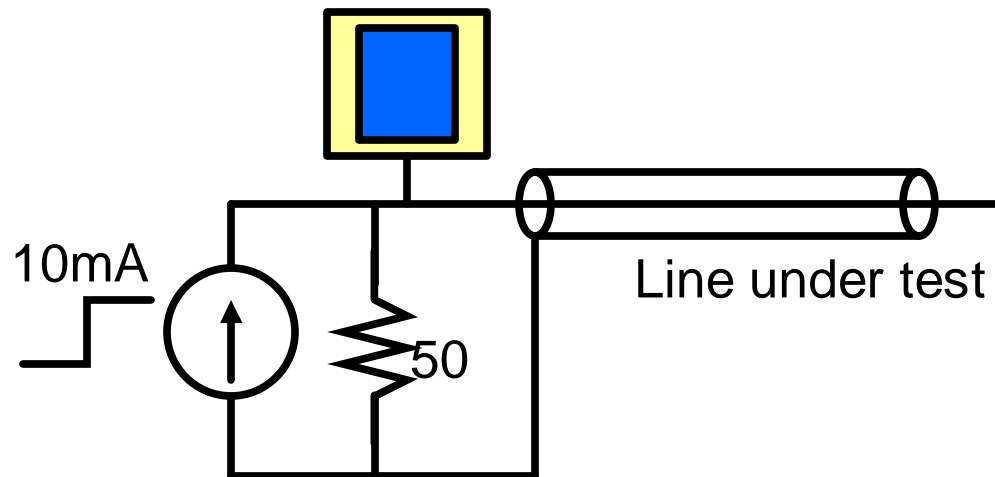
Deriving a Model

- How do we make a model of a signal path?
 - hand calculation
 - assemble models from component, connector, and package vendors
 - CAD programs
 - measurements of the actual system

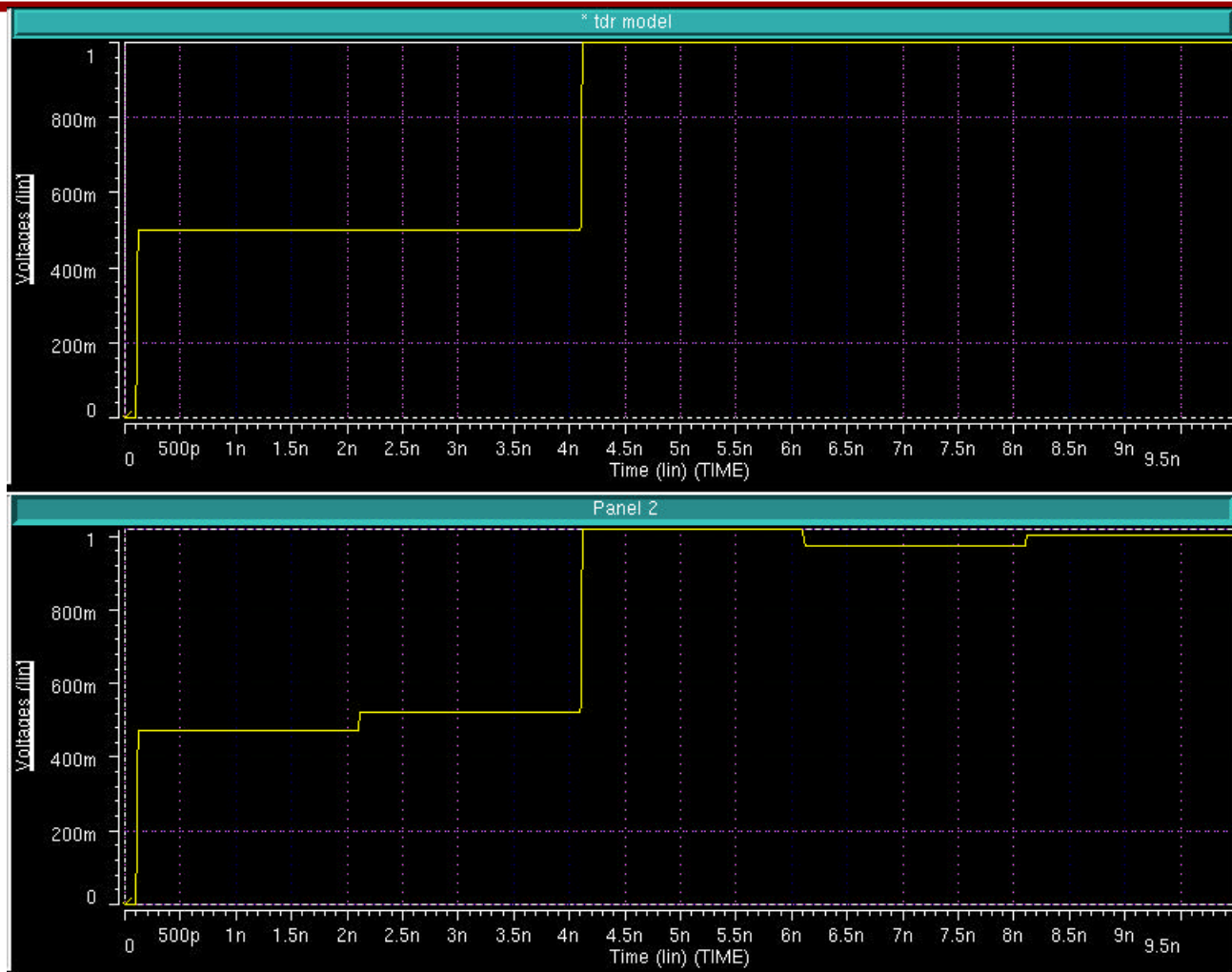


Meet the Time-Domain Reflectometer

- A time-domain reflectometer is a fast step generator and a high-speed oscilloscope.
- To characterize a line
 - inject a fast (usually 20ps) step into the line
 - observe the reflected waveform
 - what does it mean?



What made these waveforms?

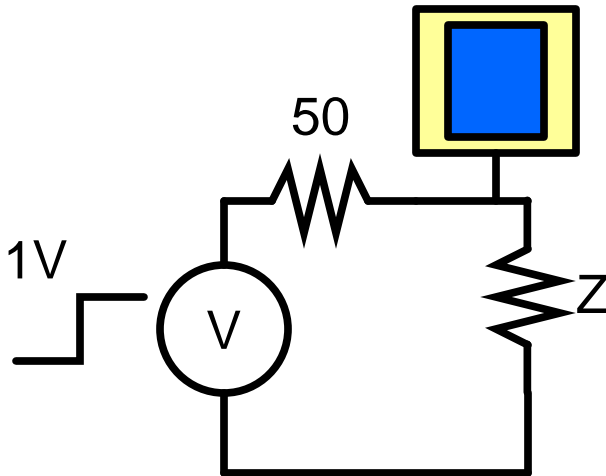


Calculating Impedance from Voltage

$$V = \frac{Z}{Z + Z_0}$$

$$(Z + Z_0)V = Z$$

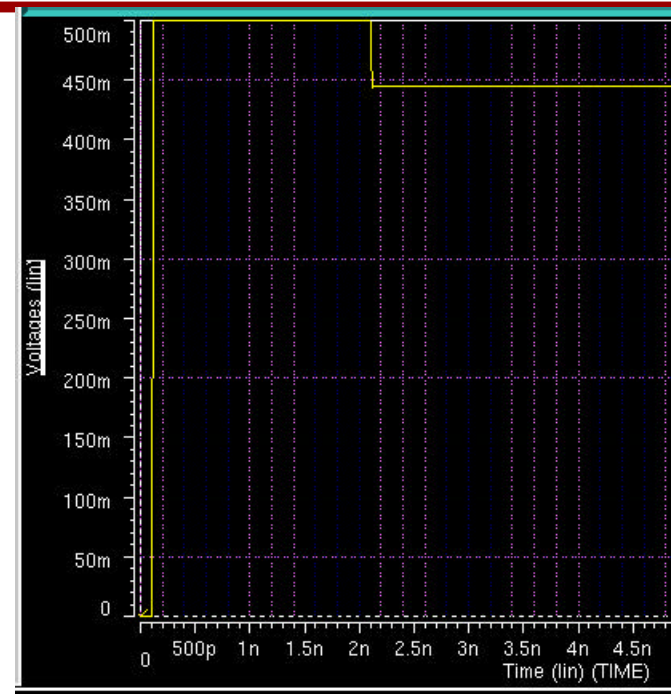
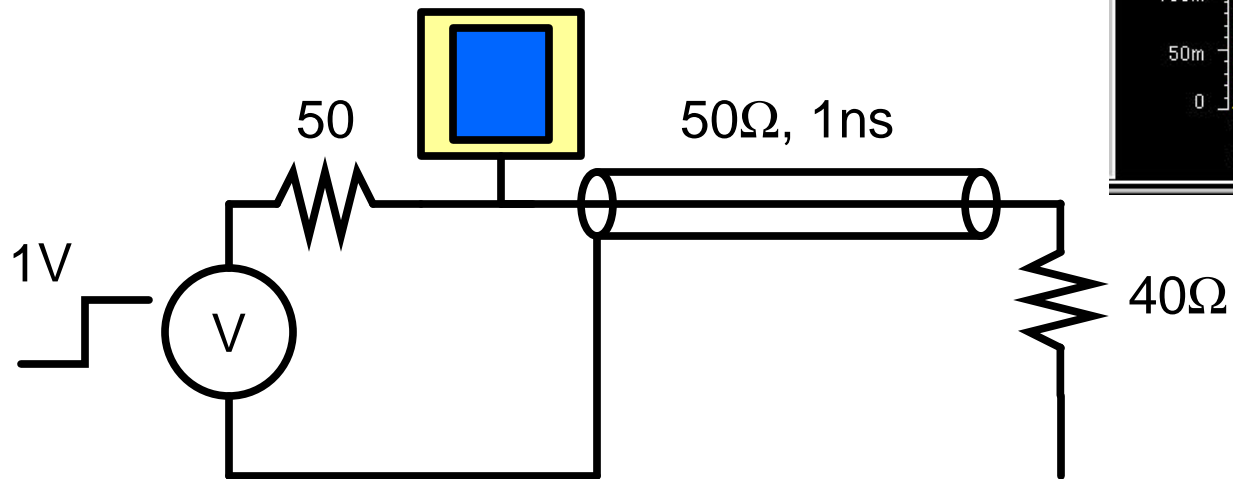
$$Z = Z_0 \left(\frac{V}{1 - V} \right)$$



V	Z
0.50	50.0
0.47	44.3
0.53	56.4

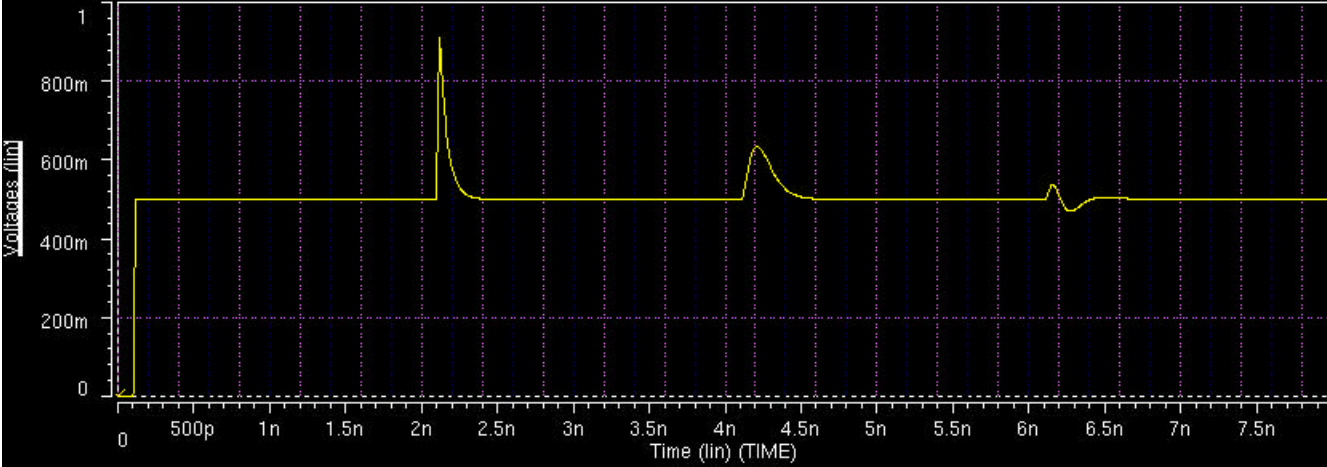
Time of Observation is Round Trip

$$Z(x) = Z_0 \left(\frac{V(2x/v)}{1 - V(2x/v)} \right)$$

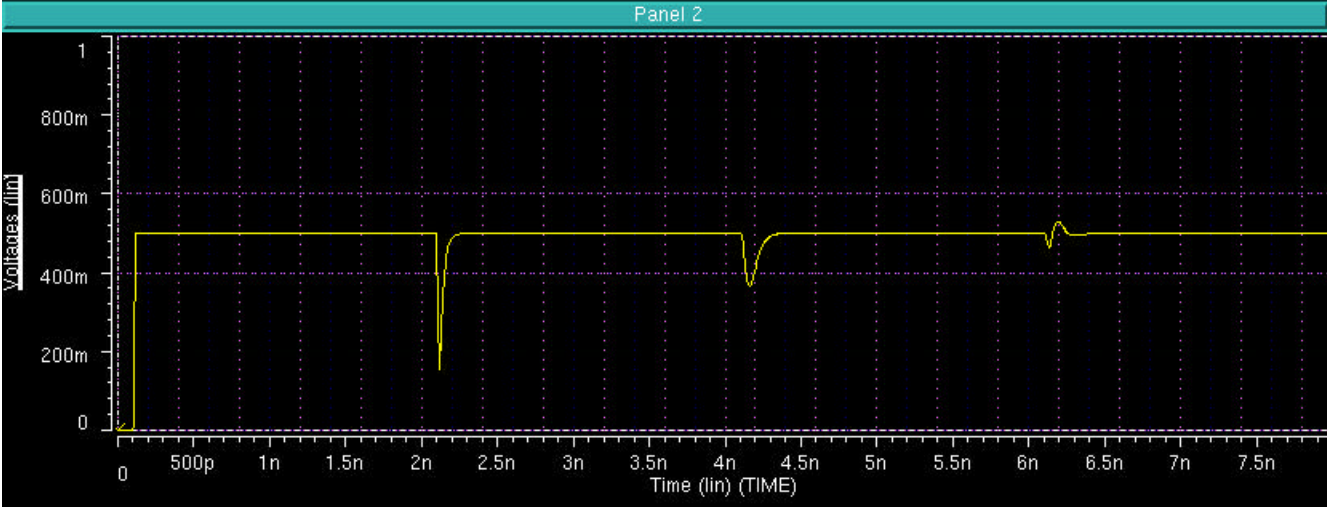


What About Inductors and Capacitors?

$$L = 2Z_0 t_L$$



$$C = \frac{2t_c}{Z_0}$$



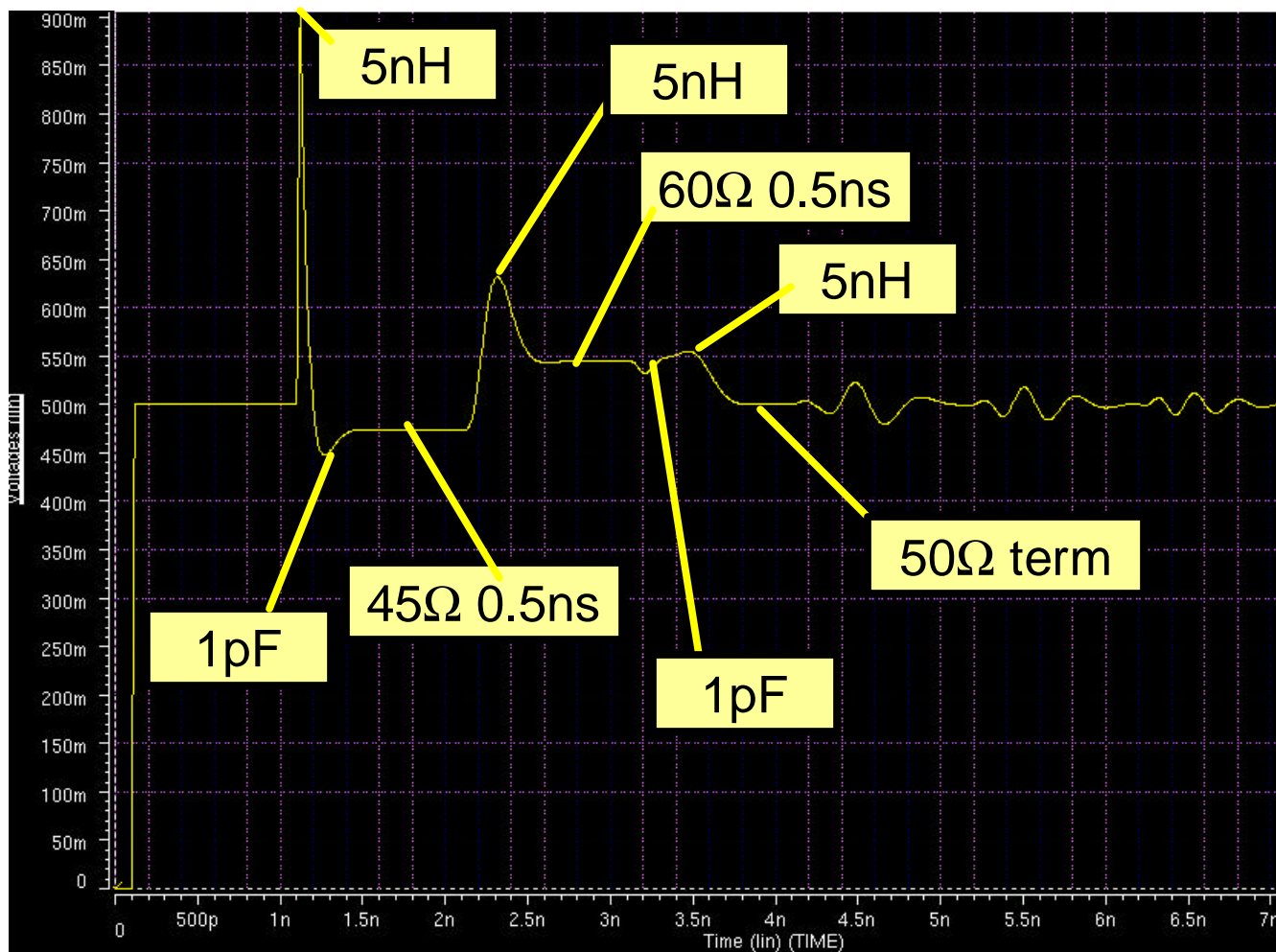
Rise-Time Degradation

- Upstream elements (Ls & Cs) low-pass the signal resulting in a longer rise-time
- This affects the reflections from down-stream elements
 - slow rising edge
 - spread out response (convolution with slow edge)
 - L & C responses don't go full swing
- This makes it
 - hard to extract exact L and C values
 - impossible to measure very small discontinuities
 - but if the TDR can't see them, neither can the signal

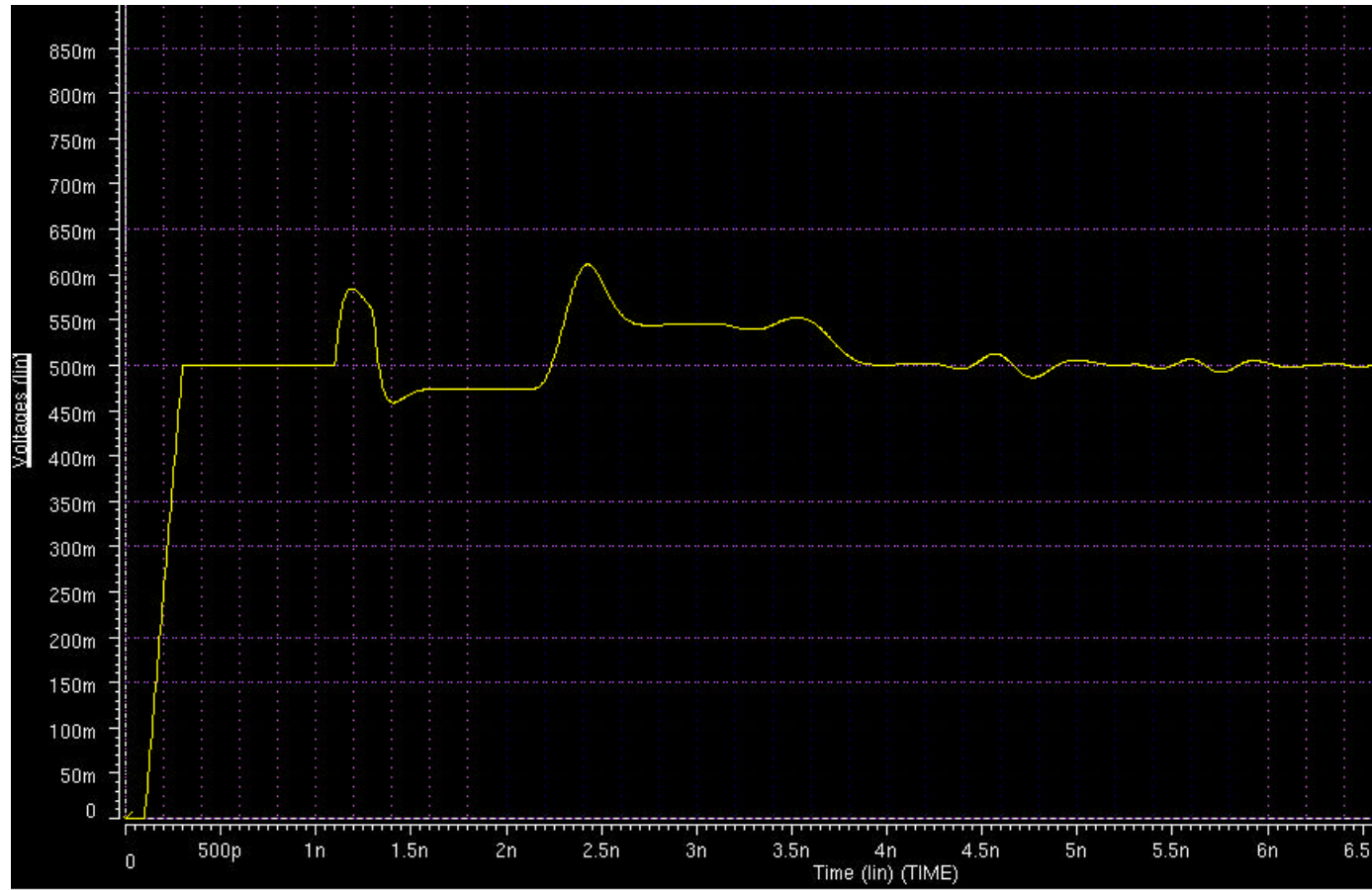
Extraction Procedure

- Identify regions of the TDR plot as
 - flat region - transmission line
 - bump up - inductor
 - bump down - capacitor
- Starting at source
 - determine value of Z & t , L , or C for nearest element
 - simulate to validate and determine new t_r
 - iterate as needed to get value right
 - move on to next element
- Don't need model with more resolution than your fastest rise time

Example TDR Trace



Same waveform with 200ps edge



Next Time

- Noise
 - what disturbs digital signals
 - fixed and proportional noise
- Power Supply Noise
 - single supply and differential
 - sources
- Cross Talk
 - capacitive crosstalk
 - transmission lines