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# EE273 Lecture 10

## Closed-Loop Timing

February 14, 2001

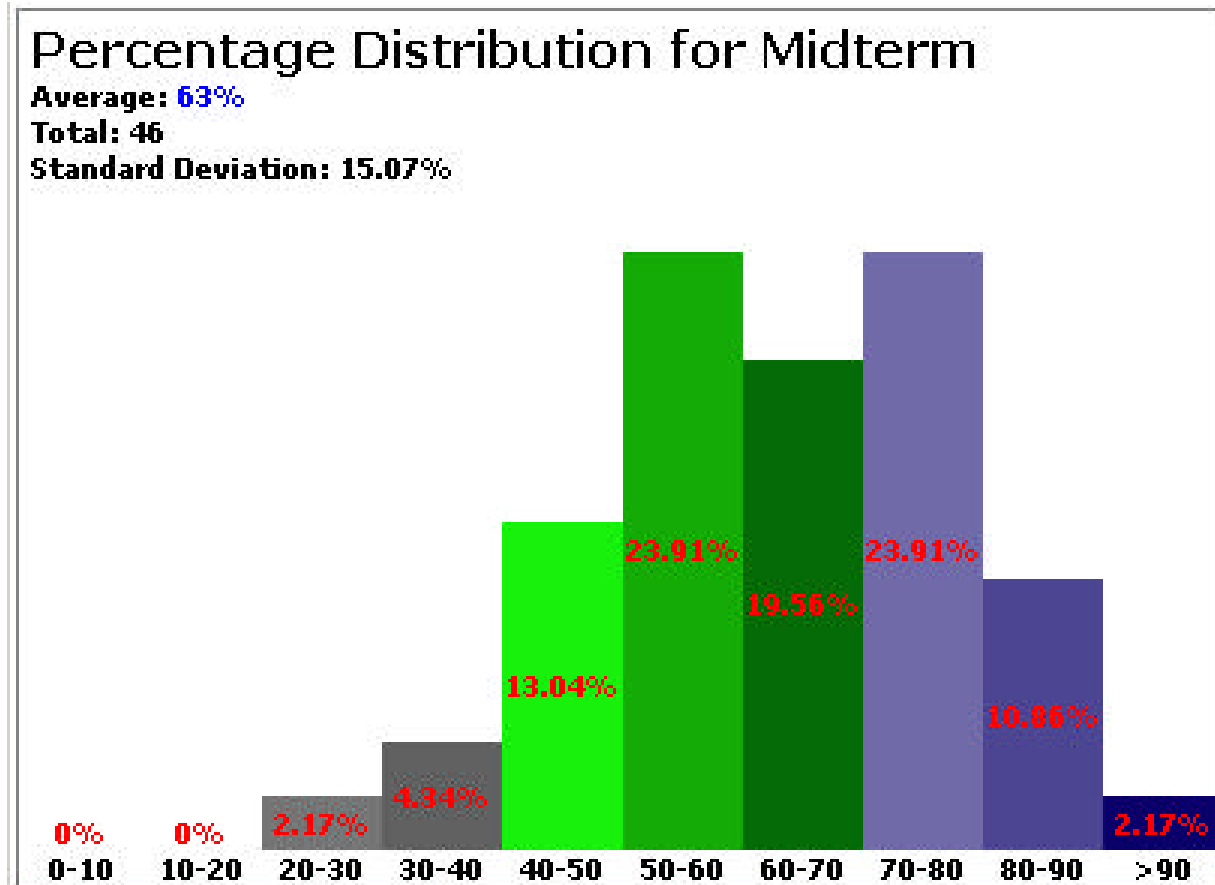
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# Logistics

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- Happy Valentine's Day!
- Midterm solution and grades are on-line
- No class on Monday 2/19
- Reading
  - Section 9.7
  - Complete before class on Wednesday 2/21
- Problem Set 5
  - 9-2, 9-3, 9-6
  - Due Wednesday 2/21
- Project Assignment
  - Available shortly
  - Due 3/7

# Midterm Histogram



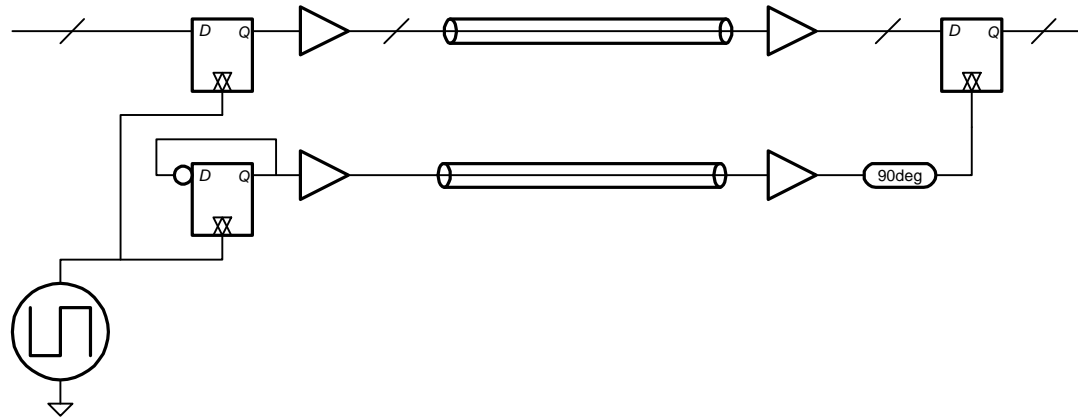
# A Quick Overview

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- Pipeline timing
  - forward clock with the data
  - eliminates ‘windows’ of operating frequencies
    - system works from DC to maximum frequency
- Closed-Loop Timing
  - skew can be eliminated by
    - measuring it
    - adding delay to compensate
  - example: a zero-delay buffer
  - components
    - phase comparator
    - variable delay line
- Bundled closed-loop timing
  - timing loop closed around one reference line
  - most sources of skew uncompensated
  - depends on matching of reference and data lines
- Per-line closed loop timing
  - timing loop closed individually around each data line
  - most sources of skew compensated

# Pipeline Timing

- Delay the clock by the same amount as the data *plus* half a bit cell
- System will work from DC to maximum frequency  $1/(t_r+t_a+t_u)$
- Defines a new clock domain at the far end of the line

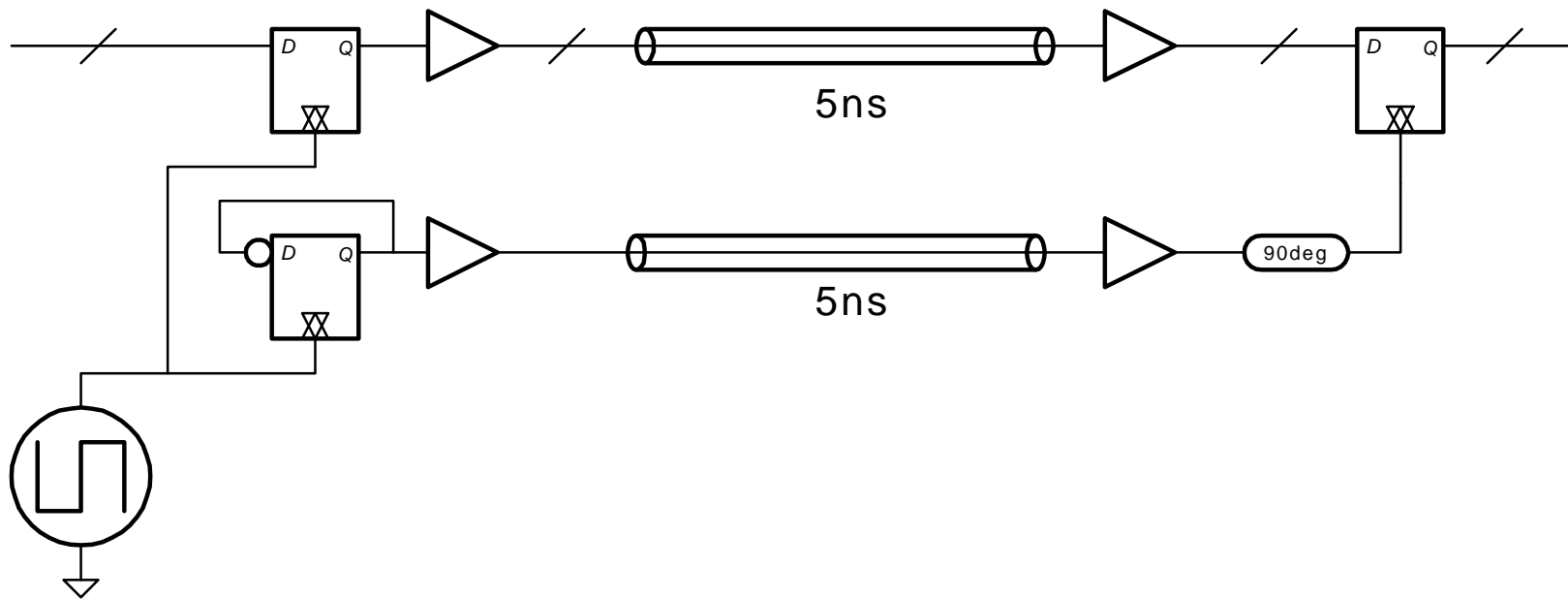


# Pipeline Timing Example

$t_r=100\text{ps}$ ,  $t_a=50\text{ps}$

$t_j=10\%$  of active delay,  $t_s=10\%$  of active delay,  $1\%$  of wire delay

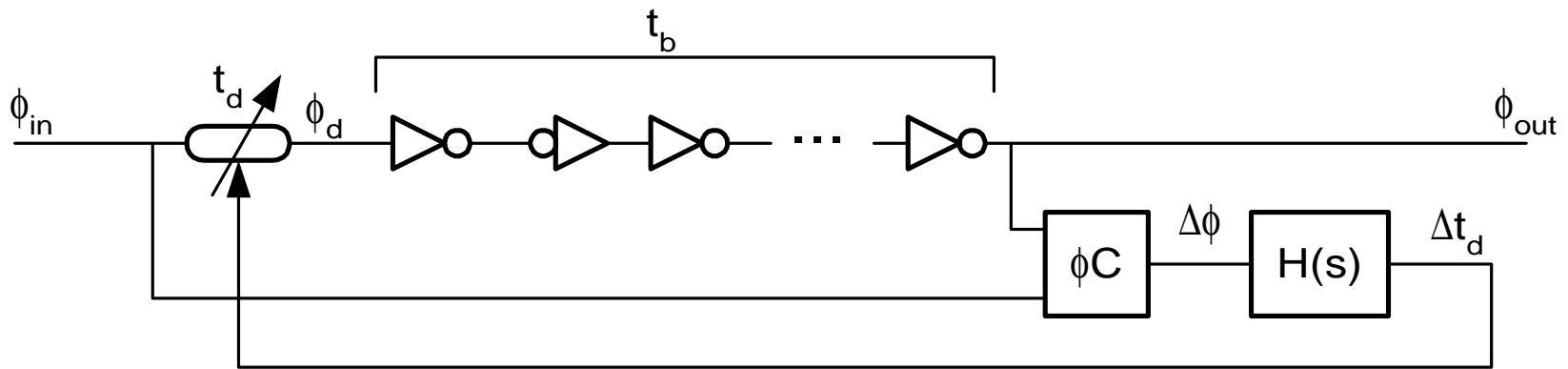
$t_{dCQ}=200\text{ps}$ ,  $t_{buf}=200\text{ps}$ ,  $t_{clk\_buf}=600\text{ps}$







# Example, a Zero-Delay Clock Buffer



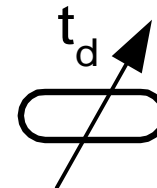
# Timing Loop Components

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- Phase Comparator
  - measures the time difference between two signal transitions
  - for periodic signals measures the phase of one signal with respect to the other
  - the sensor for most timing loops
- Delay Lines
  - adjust the delay between two points in a system
  - the actuator for most timing loops
    - except for PLLs that use VCOs
- Loop Filters
  - smooth response of the timing loop
  - stabilize the loop (for PLLs)

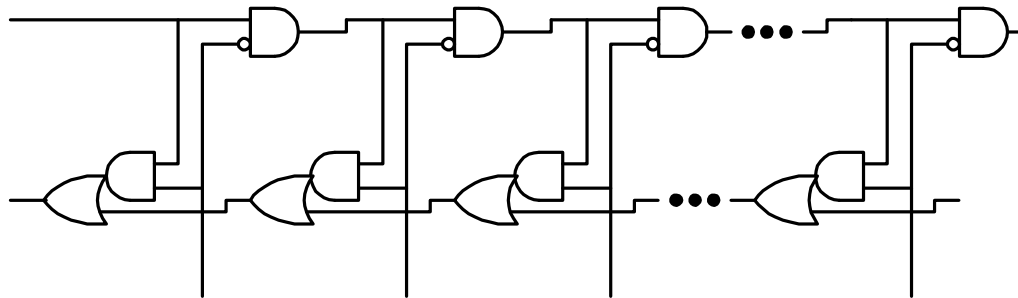
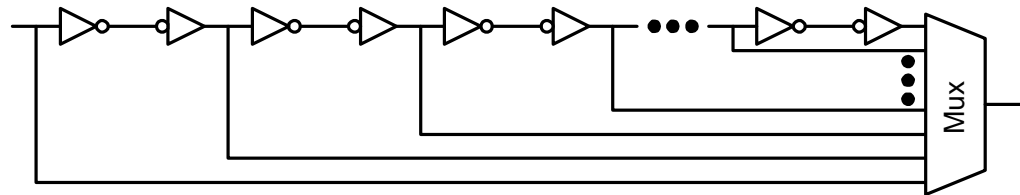
# Variable Delay Lines

- Need:
  - a delay element
  - a method to vary the delay
- Delay elements
  - inverter
  - source-coupled amplifier
- Methods to vary delay
  - multiplexing a tapped delay line
  - varying the power supply to an inverter chain
  - varying the capacitance driven by each stage
  - varying the resistive load of a source-coupled amplifier
- Characterized by
  - max and min delay
    - typically a 2:1 throw
  - stability (jitter)



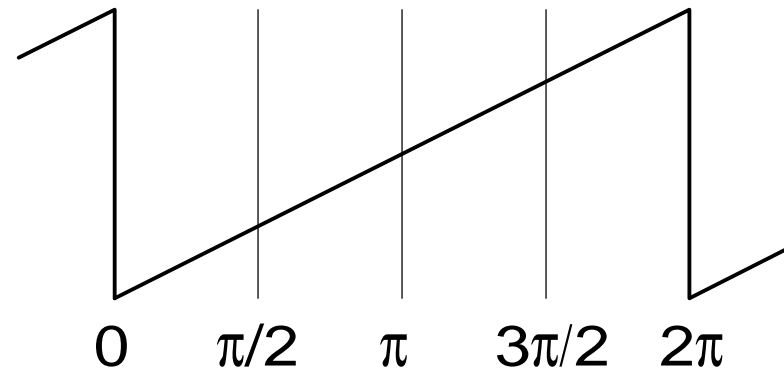
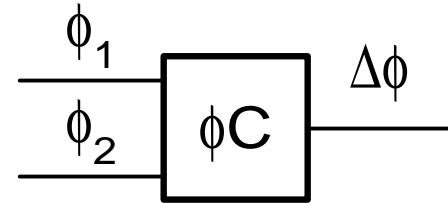
# Some All Digital Variable Delays

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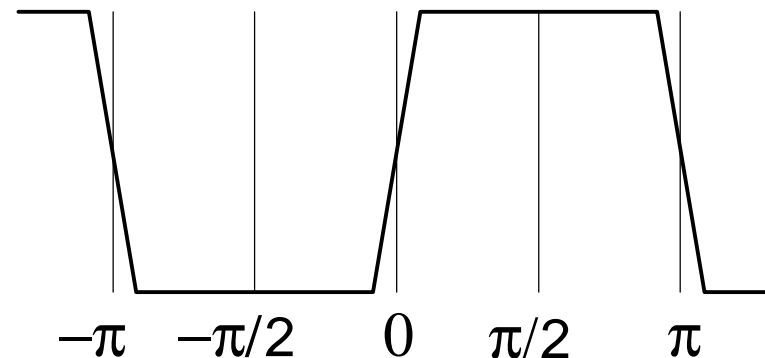
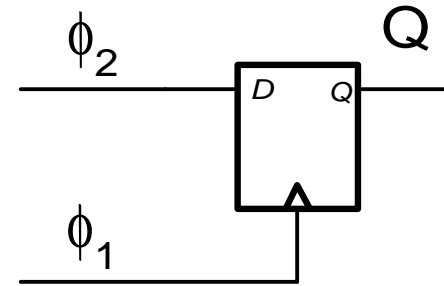
# Phase Comparators

- Output describes phase difference between two inputs
  - may be analog or digital
  - may linearly cover a wide range, or just a narrow phase difference



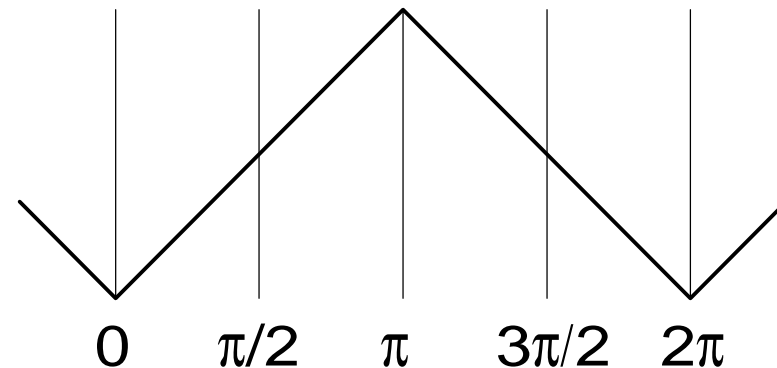
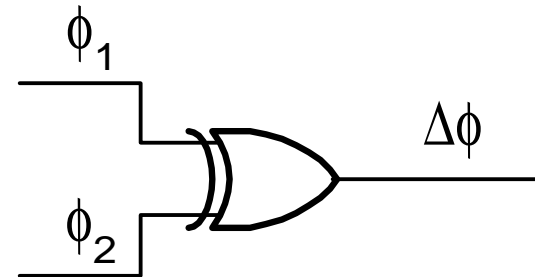
# Flip-Flop Phase Comparator

- Feed  $\phi_1$  into the clock input
- Feed  $\phi_2$  into the data input
- With single-edge triggered FF, if Q is low,  $\phi_1$  is (early late) (circle one).
- How does this work with a double-edge-triggered FF?
- Note that when  $\Delta\phi = 0$ , FF is put in a metastable state
- If same FF used for receiver and phase comparator, aperture offset is compensated for.



# Exclusive-OR Phase Comparator

- Duty factor out of comparator is proportional to phase
  - requires a low-pass filter to extract a usable value
- Wide linear range allows locking to  $\pi/2$ 
  - but low gain implies large jitter. Small voltage noise gives big phase noise.

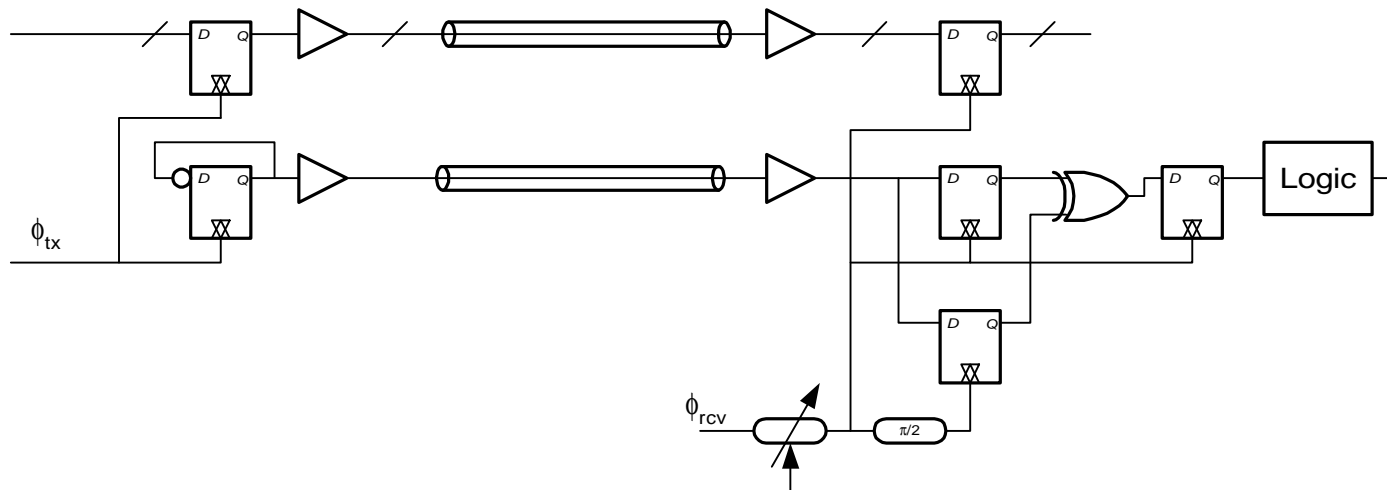


# Other Phase Comparators

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- Sequential phase-only comparator
  - asynchronous state machine
  - pulses “up” or “down” output from transition on one input to transition on the other
- Sequential phase-frequency comparator
  - like the sequential phase-only comparator
  - but also keeps track of number of transitions on the two inputs and attempts to make them equal
  - don't use this for a DLL!!!

# Link with Bundled Closed-Loop Timing

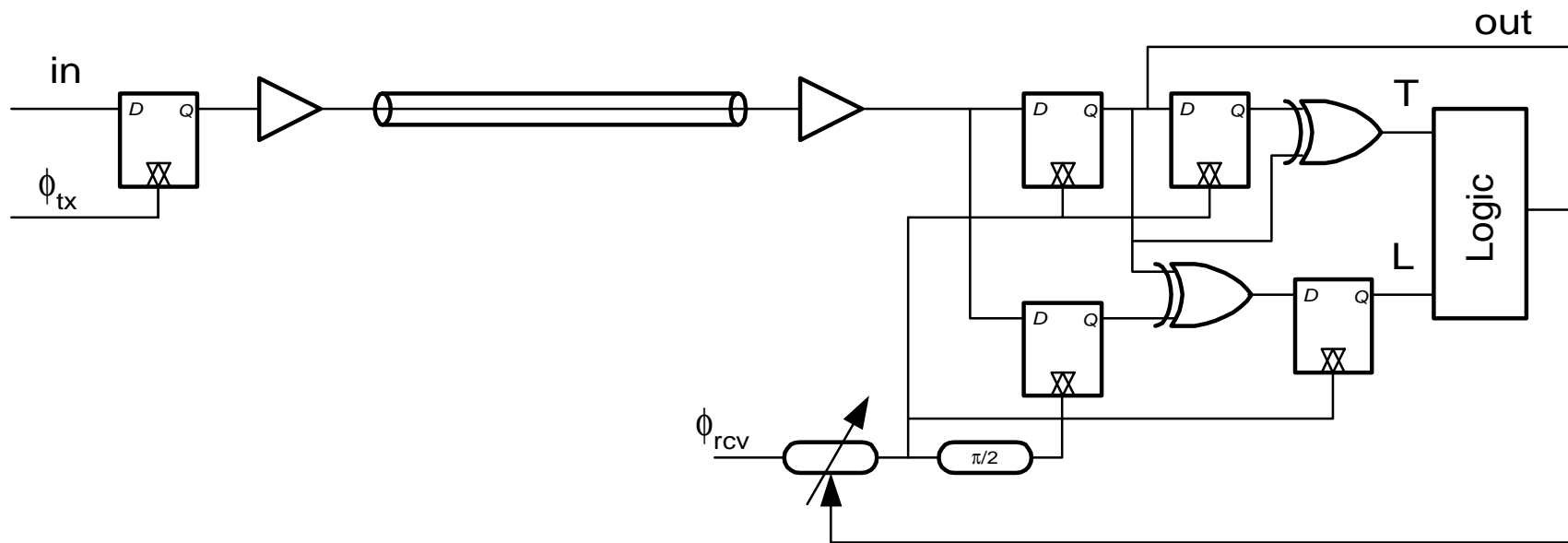


# Which of these elements of timing uncertainty are cancelled?

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- Skew
  - between clock line and data line
  - fixed differences in flip-flop, transmitter, and receiver delays
  - in transmit clock between flip-flops
  - aperture offset in receive flip flop
  - offset in 90 degree delay line
- Jitter
  - in transmit clock
  - in delay of flip-flops, transmitters, and receivers

# Link with per-line Closed-Loop Timing



# Now which of these elements of timing uncertainty are cancelled?

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- Skew

- between clock line and data line
- fixed differences in flip-flop, transmitter, and receiver delays
- in transmit clock between flip-flops
- aperture offset in receive flip flop
- offset in 90 degree delay line

- Jitter

- in transmit clock
- in delay of flip-flops, transmitters, and receivers

# Next Time

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- Clock Distribution