EE273 Lecture 14
Off-Chip Power Distribution
March 5, 2001

William J. Dally
Computer Systems Laboratory
Stanford University
billd@csl.stanford.edu
Logistics

• Project
  – Due Wednesday 3/7
  – Automatic extension until 3/12

• Reading
  – Sections 5.3 and 5.4

• Final Exam
  – Friday 3/23, 8:30AM to 10:30AM
  – Location TBD

• Upcoming Lecture Schedule
  – 3/7 – Power distribution – on-chip and summary
  – 3/12 – Wrapup
  – 3/14 – Guest lecture
A Quick Overview

• The Power-Distribution Problem
  – DC supply voltage with small tolerance
  – AC current, large di/dt
  – Inductive and resistive supply components

• Inductive Power Supply Noise
  – L supplies low-frequency current, C supplies high frequency
  – ripple due to current variation within each cycle
  – transient at start/stop of load current

• Bypass Capacitors
  – parasitic L and R in capacitors make them effective only below a certain frequency

• Local Regulation
  – series and parallel (shunt)
  – clip voltage ripple
  – ‘subtract’ AC current
  – distribute at a more convenient voltage
The Power Distribution Problem

- Modern digital systems operate at small DC voltages
  - 1.2 to 3.3V
  - must be held to within ±10% (or less)
- and draw large AC currents
  - 10A or more per chip, 100A per board, KA in a system
  - may go from 0 to full current in less than one clock cycle
- over a supply network with parasitic elements
  - Inductance of bus bars, PC boards, packages, and bond wires
  - Resistance of on-chip wires
A Typical Power Supply Network

- Actually a tree with branching at each level
- Parasitic inductance (off-chip) and resistance (on-chip)
- Power and ground networks are usually symmetric
- Capacitance added to give a *tapered* frequency response
Typical Load Current

- For a given clock domain, load is usually periodic with the clock
- May stop or start in a single clock cycle
- With multiple clock domains, they may drift into phase reinforcing one another

- Load is often resistive, varying linearly with supply voltage
- Some loads are high impedance, constant independent of supply voltage
Local Loads and Signal Loads

- Logic loads connect a point in the power network to a corresponding point in the ground network
  - current can be supplied from a nearby bypass capacitor
- Signal loads connect a point in the power network to a distant point in the ground network
  - usually due to unbalanced signaling
  - current must return over a long path
  - bypass capacitors are not effective
Inductive Supply Noise

- Each section of the supply network is an LC circuit
  - has a resonant frequency, \( \omega_{LC} = (LC)^{-1/2} \)
  - inductor carries DC current (\(\ll \omega_{LC}\))
  - capacitor supplies AC current (\(\gg \omega_{LC}\))
- Size capacitor to
  - supply cycle to cycle AC current with acceptable ripple
  - handle inductor start/stop transient
Response of an LC Section to Typical Supply Current

L = 4e-008 C=1e-008

Load Current, IL

Inductor Current, I_l

Capacitor Voltage, V_L
Magnitude of Ripple within a Cycle

- Over a clock cycle, inductor current is essentially constant, $I_{\text{avg}}$
- Load current varies considerably
- Capacitor current is the difference
- Capacitor voltage *ripples* due to this AC current

\[
\Delta V = \frac{k_i I_{\text{avg}} t_{ck}}{C_B}
\]

\[
C_B > \frac{k_i I_{\text{avg}} t_{ck}}{\Delta V_{\text{max}}}
\]
Starting and Stopping on a Dime

- When circuit is off, inductor current is 0.
- During startup, the capacitor must supply current to the load while the inductor current ramps up.
- Similarly, when the circuit shuts down, the capacitor must absorb the inductor current while it ramps down.
- In either case, the situation is that of a step current into an LC circuit.
- Response is a sine-wave.

\[
\Delta V = \frac{I_{\text{avg}}}{C_B \omega_C} \sin(\omega_c t)
\]

\[
= I_{\text{avg}} \sqrt{\frac{L}{C}} \sin(\omega_c t)
\]

\[
\Delta V_{\text{max}} = I_{\text{avg}} \sqrt{\frac{L}{C}}
\]
Bypass Capacitor to Handle Start/Stop Transient

\[
\Delta V_{\text{max}} = I_{\text{avg}} \sqrt{\frac{L}{C_B}}
\]

\[
C_B > \left( \frac{I_{\text{avg}}}{\Delta V_{\text{peak}}} \right)^2 L
\]

\[
L_{i+1} < C_i \left( \frac{\Delta V_{\text{peak}}}{I_{\text{avg}}} \right)^2
\]
Sizing Bypass Capacitors

- Bypass capacitor must be sized to handle both types of inductive power supply noise
  - ripple due to non-uniform current within a clock cycle
  - start/stop transients
  - maximum ripple can happen at peak or trough of transient
- Approximate capacitance requirement by summing the independent requirements
- Usually several stages are required to meet both constraints

\[
\Delta V_{\text{max}} = I_{\text{avg}} \sqrt{\frac{L}{C_B}} + \frac{k_i I_{\text{avg}} t_{ck}}{C_B}
\]

\[
C_B > \left( \frac{I_{\text{avg}}}{\Delta V_{\text{max}}} \right)^2 L + \frac{k_i I_{\text{avg}} t_{ck}}{\Delta V_{\text{max}}}
\]

\[
C_B > \left( \frac{I_{\text{avg}}}{\Delta V_{\text{max}}} \right) \left( k_i t_{ck} + \frac{I_{\text{avg}}}{\Delta V_{\text{max}}} L \right)
\]
The Truth about Bypass Capacitors

- Most capacitors are only capacitors at low frequencies
- Capacitors have parasitic series resistance and inductance
- Every pico-Farad has its very own nano-Henry
- Two key breakpoints
  - LC frequency
  - RC frequency
- Capacitors are ineffective at bypassing currents above *either* of these frequencies
Impedance vs. Frequency for some Typical Capacitors

- $C = 10\mu F, L=10nH, R=1$
- $C = 10nF, L=5nH, R=0.1$
### Capacitor Properties

<table>
<thead>
<tr>
<th>Type</th>
<th>C</th>
<th>R</th>
<th>L</th>
<th>(f_{RC})</th>
<th>(f_{LC})</th>
<th>(f_{LR})</th>
</tr>
</thead>
<tbody>
<tr>
<td>On-chip MOS</td>
<td>250fF</td>
<td>10</td>
<td>0</td>
<td>64GHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>On-chip MOS</td>
<td>1pF</td>
<td>40</td>
<td>0</td>
<td>4GHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMT ceramic</td>
<td>1pF</td>
<td>0.1</td>
<td>1nH</td>
<td></td>
<td>160MHz</td>
<td></td>
</tr>
<tr>
<td>SMT ceramic</td>
<td>1nF</td>
<td>0.1</td>
<td>1nH</td>
<td></td>
<td>50MHz</td>
<td></td>
</tr>
<tr>
<td>Ceramic disk</td>
<td>10nF</td>
<td>0.1</td>
<td>5nH</td>
<td></td>
<td>23MHz</td>
<td></td>
</tr>
<tr>
<td>Al Electrolytic</td>
<td>10(\mu)F</td>
<td>1</td>
<td>10nH</td>
<td>160KHz</td>
<td></td>
<td>16MHz</td>
</tr>
<tr>
<td>Al Electrolytic</td>
<td>1mF</td>
<td>0.05</td>
<td>10nH</td>
<td>3KHz</td>
<td></td>
<td>800KHz</td>
</tr>
</tbody>
</table>

- High frequency is only achieved with small capacitors
- Many capacitors can be used in parallel to increase capacitance without reducing frequency
Special Low L Capacitors Do Substantially Better
Bypass Network Design Procedure

1. Start at the load and work out
2. At each stage, i
   1. Size the capacitance to handle the HF current $C_i > k_i t/\Delta V$
   2. Size the capacitor as big as possible (economically) while keeping the inductance $L_i$ small enough for the transient limit of the previous stage (i-1)
3. Done when capacitance is greater than $L_s(I/\Delta V)$

Really picking capacitors based on their inductance
Example Design

- One chip, 10A, $t_{ck} = 2\text{ns}$, $k = 0.5$, $\Delta V = 0.1\text{V}$, $\frac{di}{dt} = \frac{40\text{A}}{0.5\text{ns}} = 80\text{GA/s}$, $L_s = 100\text{nH}$

- First rank
  - $C_1 > \frac{(0.5 \times 10 \times 2\text{ns})}{0.1} = 100\text{nF}$
  - $L_1 < \frac{\Delta V}{\frac{di}{dt}} = \frac{0.1}{80\text{G}} = 1.25\text{pH}$
  - Choose on-chip 250nF capacitor
    - Could get by with 100nF, but 250nF makes the next level easier

- Second Rank
  - $L_2 < C_1(\Delta V/I)^2 = 250\text{n}(0.1/10)^2 = 0.025\text{nH}$
    - First rank increases inductance limit by 20x (would have been 8x with 100nF)
  - Choose 10 2.2µF IDC caps (175pH each) on package
    - And lots (100s) of solder balls to keep total L less than 25pH
Example Design (cont)

- **Third Rank**
  - \( L_3 < C_2(\Delta V/I)^2 = 22\mu(0.1/10)^2 = 2.2\text{nH} \)
  - Choose 5 1000\( \mu \)F Ultra low ESR Tantalum capacitors
    - ESR of 0.018\( \Omega \) each, 0.0036\( \Omega \) total.
    - Current rating of 2.1A – 10.5A total
    - 0.036V ripple with 10A current
  - We’re done since \( C_3 = 5000\mu\text{F} > L_s(I/\Delta V)^2 = 100n \times (10/.1)^2 \)
    \( = 1000\mu\text{F} \)
A Typical Tantalum
Local Power Supply Regulation

- Can put a regulator in series or parallel with the power supply
- Parallel or *shunt* regulators control current
  - add a current to the AC load current to make it look more like a DC current
- Series regulators control voltage
  - clip off the top of the voltage ripple and transient response
  - distribute power at a higher voltage (or AC voltage)
Shunt Regulators and Clamps

- Shunt regulators maintain a steady current draw from the distribution network
  - Measure the load current, \( I_L \)
  - Generate a shunt current \( I_R = I_{\text{max}} - I_L \)
  - Current is now DC
    - but large
- A clamp handles the turn-off transient to avoid overvoltage
  - measure the load voltage, \( V_C \)
  - draw current when \( V_C \) exceeds a threshold
Series Linear Regulators

- Think of the regulator as a variable series resistor
  - drop distribution voltage (e.g., 3.3V) down to a load voltage (e.g., 2.5V)
- Can clip off the top of the voltage ripple by resistively dropping it
- Limited by
  - frequency response of the regulator (can’t track fast transients)
  - series nature of regulator, can’t divert transient inductor current
Switching Regulators

- A *switching* regulator uses a reactive element (usually a transformer or inductor) to convert the supply from one voltage to another with only a small loss in power.

- Distributing power at a high voltage improves things quadratically:
  - less current to distribute
  - more voltage to tolerate ripple

- Often advantageous to make this distribution voltage AC (at 0.1kHz to 1MHz)

\[
\begin{align*}
V_D &= kV_P \\
I_D &= \frac{I_P}{k} \\
\frac{\Delta V_D}{V_D} &= \frac{Z_D I_D}{V_D} \quad \Rightarrow \quad \frac{Z_D I_P}{k^2 V_P}
\end{align*}
\]
Next Time

- On-Chip Power Distribution