EE273 Lecture 14
Off-Chip Power Distribution

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Logistics

- Project
  - Due Wednesday 3/7
  - Automatic extension until 3/12
- Reading
  - Sections 5.3 and 5.4
- Final Exam
  - Friday 3/23, 8:30AM to 10:30AM
  - Location TBD
- Upcoming Lecture Schedule
  - 3/7 – Power distribution – on-chip and summary
  - 3/12 – Wrapup
  - 3/14 – Guest lecture

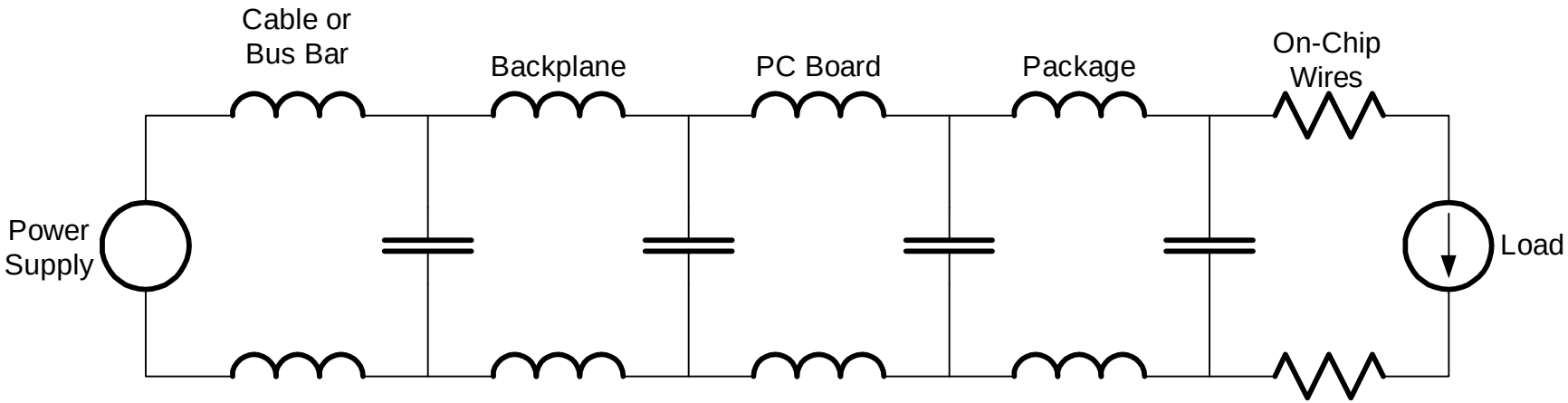
A Quick Overview

- The Power-Distribution Problem
  - DC supply voltage with small tolerance
  - AC current, large di/dt
  - Inductive and resistive supply components
- Inductive Power Supply Noise
  - L supplies low-frequency current, C supplies high frequency
  - ripple due to current variation within each cycle
  - transient at start/stop of load current
- Bypass Capacitors
  - parasitic L and R in capacitors make them effective only below a certain frequency
- Local Regulation
  - series and parallel (shunt)
  - clip voltage ripple
  - ‘subtract’ AC current
  - distribute at a more convenient voltage

The Power Distribution Problem

- Modern digital systems operate at small DC voltages
  - 1.2 to 3.3V
  - must be held to within ±10% (or less)
- and draw large AC currents
  - 10A or more per chip, 100A per board, KA in a system
  - may go from 0 to full current in less than one clock cycle
- over a supply network with parasitic elements
  - Inductance of bus bars, PC boards, packages,and bond wires
  - Resistance of on-chip wires

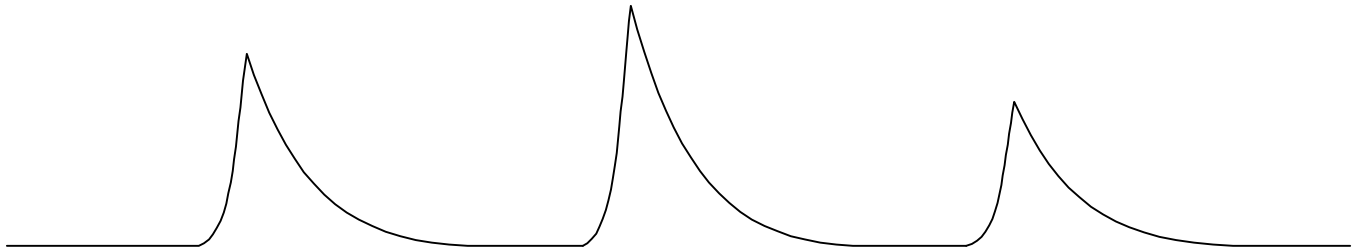
A Typical Power Supply Network



- Actually a tree with branching at each level
- Parasitic inductance (off-chip) and resistance (on-chip)
- Power and ground networks are usually symmetric
- Capacitance added to give a *tapered* frequency response

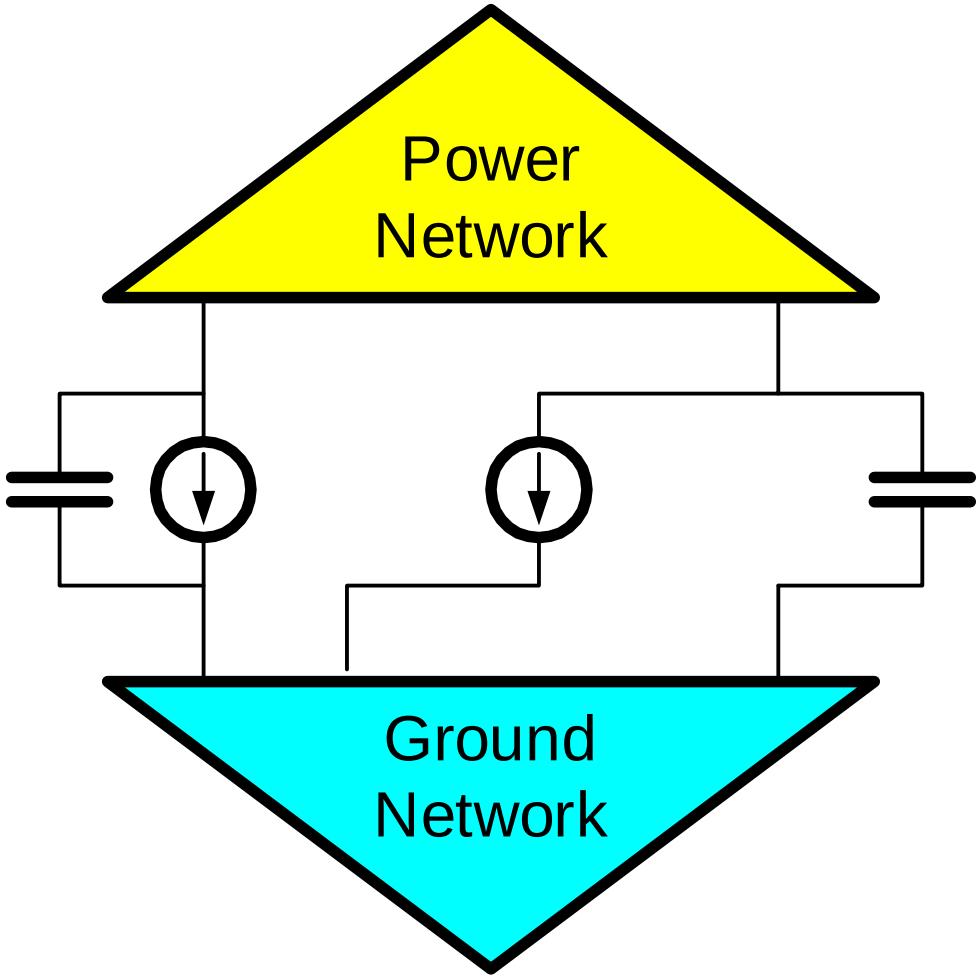
Typical Load Current

- For a given clock domain, load is usually periodic with the clock
- May stop or start in a single clock cycle
- With multiple clock domains, they may drift into phase reinforcing one another
- Load is often *resistive*, varying linearly with supply voltage
- Some loads are *high impedance,* constant independent of supply voltage



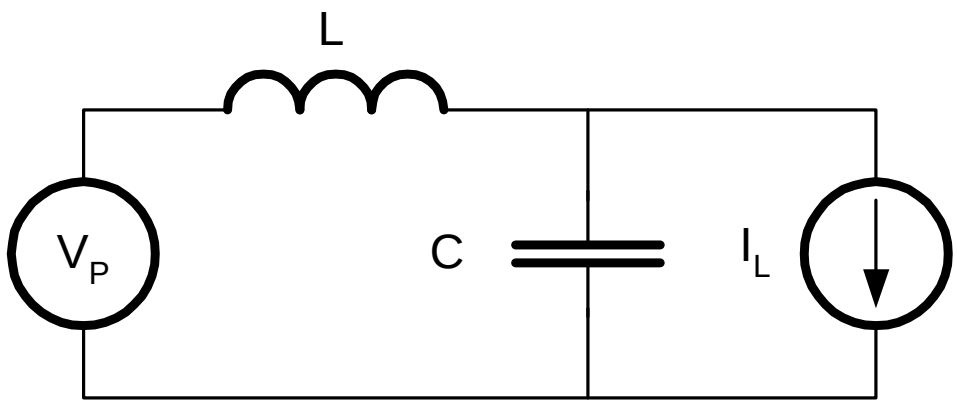
Local Loads and Signal Loads

- Logic loads connect a point in the power network to a corresponding point in the ground network
  - current can be supplied from a nearby bypass capacitor
- Signal loads connect a point in the power network to a distant point in the ground network
  - usually due to unbalanced signaling
  - current must return over a *long* path
  - bypass capacitors are not effective

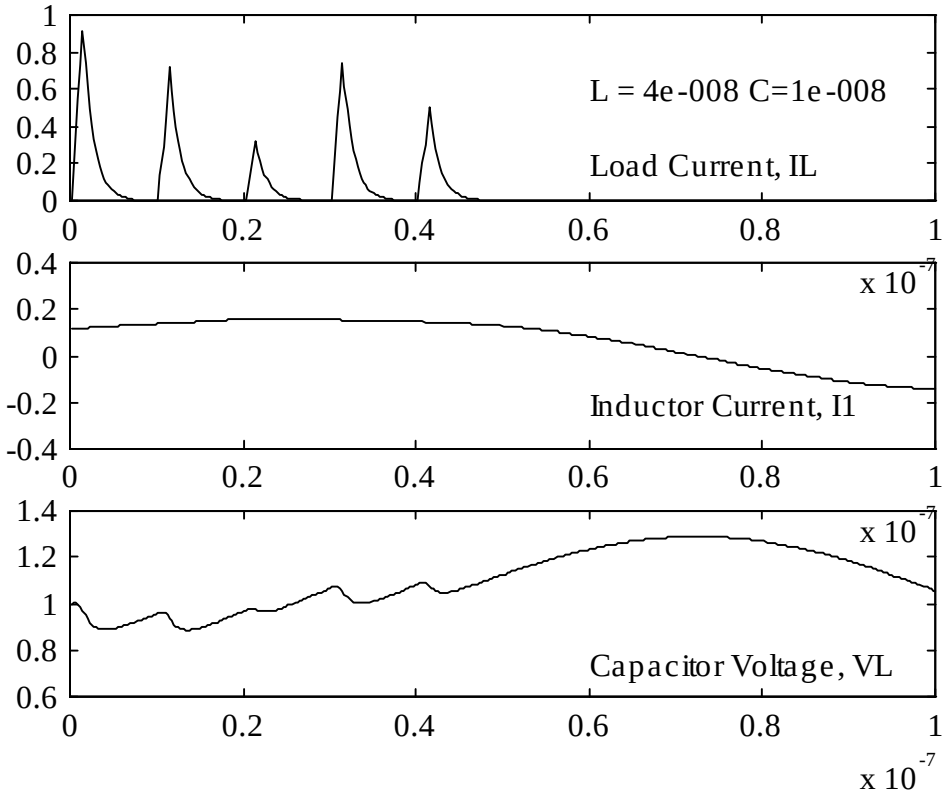


Inductive Supply Noise

- Each section of the supply network is an LC circuit
  - has a resonant frequency, $\omega_{LC} = (LC)^{-1/2}$
  - inductor carries DC current ($<< \omega_{LC}$)
  - capacitor supplies AC current ($>> \omega_{LC}$)
- Size capacitor to
  - supply cycle to cycle AC current with acceptable ripple
  - handle inductor start/stop transient



Response of an LC Section to Typical Supply Current



Magnitude of Ripple within a Cycle

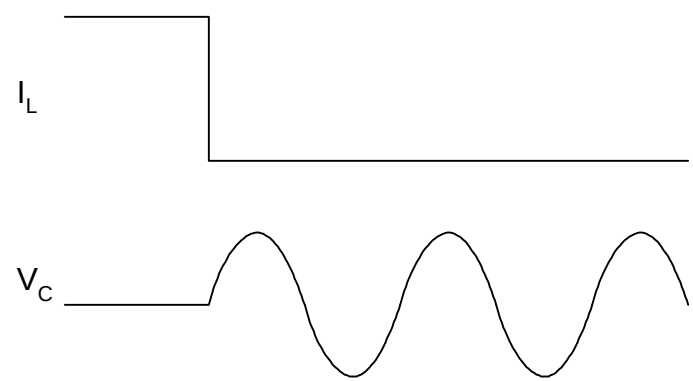
- Over a clock cycle, inductor current is essentially constant, I_{avg}
- Load current varies considerably
- Capacitor current is the difference
- Capacitor voltage *ripples* due to this AC current

$$\Delta V = \frac{k_i I_{\text{avg}} t_{ck}}{C_B}$$

$$C_B > \frac{k_i I_{\text{avg}} t_{ck}}{\Delta V_{\max}}$$

Starting and Stopping on a Dime

- When circuit is *off*, inductor current is 0.
- During startup, the capacitor must supply current to the load while the inductor current ramps up
- Similarly, when the circuit shuts down, the capacitor must absorb the inductor current while it ramps down
- In either case, the situation is that of a step current into an LC circuit
- Response is a sine-wave

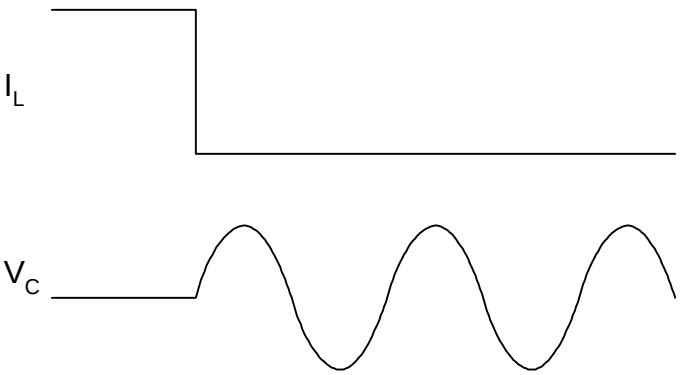


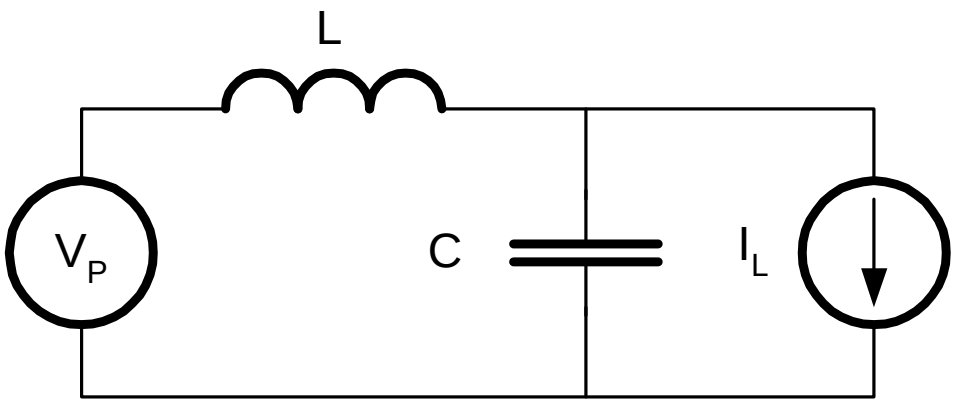
$$\Delta V = \frac{I_{\text{avg}}}{C_B w_C} \sin(w_C t)$$

$$= I_{\text{avg}} \sqrt{\frac{L}{C}} \sin(w_C t)$$

$$\Delta V_{\max} = I_{\text{avg}} \sqrt{\frac{L}{C}}$$

Bypass Capacitor to Handle Start/Stop Transient





$$\Delta V_{\max} = I_{\text{avg}} \sqrt{\frac{L}{C_B}}$$

$$C_B > \left(\frac{I_{\text{avg}}}{\Delta V_{\text{peak}}} \right)^2 L$$

$$L_{i+1} < C_i \left(\frac{\Delta V_{\text{peak}}}{I_{\text{avg}}} \right)^2$$

Sizing Bypass Capacitors

- Bypass capacitor must be sized to handle both types of inductive power supply noise
  - ripple due to non-uniform current within a clock cycle
  - start/stop transients
  - maximum ripple can happen at peak or trough of transient
- Approximate capacitance requirement by summing the independent requirements
- Usually several *stages* are required to meet both constraints

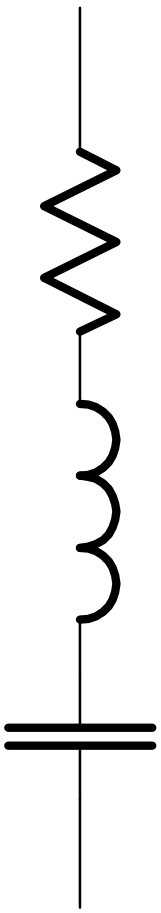
$$\Delta V_{\max} = I_{\text{avg}}\sqrt{\frac{L}{C_B}} + \frac{k_i I_{\text{avg}} t_{ck}}{C_B}$$

$$C_B > \left(\frac{I_{\text{avg}}}{\Delta V_{\max}}\right)^2 L + \frac{k_i I_{\text{avg}} t_{ck}}{\Delta V_{\max}}$$

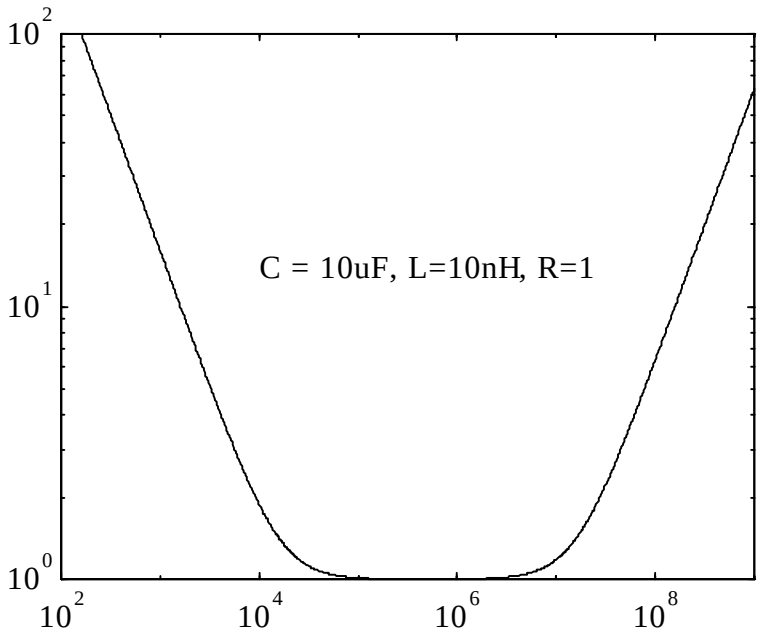
$$C_B > \left(\frac{I_{\text{avg}}}{\Delta V_{\max}}\right)\left(k_i t_{ck} + \left(\frac{I_{\text{avg}}}{\Delta V_{\max}}\right)L\right)$$

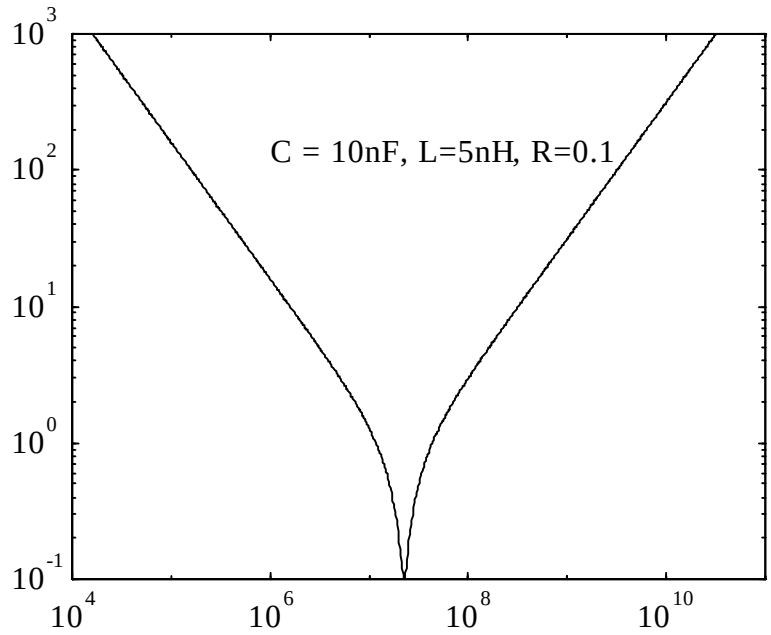
The Truth about Bypass Capacitors

- Most capacitors are only capacitors at low frequencies
- Capacitors have parasitic series resistance and inductance
- Every pico-Farad has its very own nano-Henry
- Two key breakpoints
  - LC frequency
  - RC frequency
- Capacitors are ineffective at bypassing currents above *either* of these frequencies



Impedance vs. Frequency for some Typical Capacitors



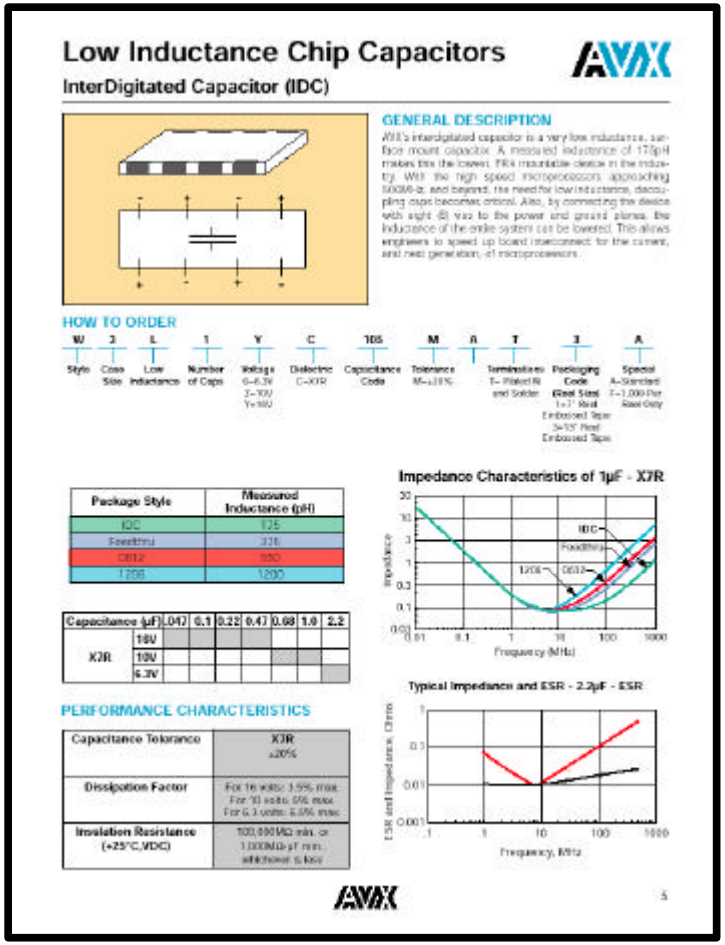


Capacitor Properties

Type	C	R	L	f_{RC}	f_{LC}	f_{LR}
On-chip MOS	250fF	10	0	64GHz		
On-chip MOS	1pF	40	0	4GHz		
SMT ceramic	1pF	0.1	1nH		160MHz	
SMT ceramic	1nF	0.1	1nH		50MHz	
Ceramic disk	10nF	0.1	5nH		23MHz	
Al Electrolytic	10μF	1	10nH	160KHz		16MHz
Al Electrolytic	1mF	0.05	10nH	3KHz		800KHz

- High frequency is only achieved with small capacitors
- Many capacitors can be used in parallel to increase capacitance without reducing frequency

Special Low L Capacitors Do Substantially Better



Low Inductance Chip Capacitors

AVX

InterDigitated Capacitor (IDC)

GENERAL DESCRIPTION

AVX's interdigitated capacitor is a very low inductance, surface mount capacitor. A measured inductance of 175pH makes this the lowest, PRA mountable device in the industry. With the high speed microprocessors approaching 500MHz and beyond, the need for low inductance, decoupling caps becomes critical. Also, by connecting the device with eight (8) vias to the power and ground planes, the inductance of the entire system can be lowered. This allows engineers to speed up board interconnect for the current, and next generation, of microprocessors.

HOW TO ORDER

W	3	L	1	Y	C	105	M	A	T	3	A
Style	Case Size	Low Inductance	Number of Caps	Voltage 6=6.3V 2=10V Y=16V	Dielectric C=X7R	Capacitance Code	Tolerance M=±20%		Terminations T=Plated Ni and Solder	Packaging Code (Reel Size) 1=7" Reel Embossed Tape 3=13" Reel Embossed Tape	Special A=Standard Z=1,000 Per Reel Only

Package Style	Measured Inductance (pH)
IDC	175
Feedthru	325
0612	550
1206	1200

Capacitance (µF)		.047	0.1	0.22	0.47	0.68	1.0	2.2
X7R	16V							
	10V							
	6.3V							

Impedance Characteristics of 1µF - X7R

Typical Impedance and ESR - 2.2µF - ESR

PERFORMANCE CHARACTERISTICS

Capacitance Tolerance	X7R ±20%
Dissipation Factor	For 16 volts: 3.5% max. For 10 volts: 5% max. For 6.3 volts: 6.5% max.
Insulation Resistance (+25°C,VDC)	100,000MΩ min. or 1,000MΩ-µF min., whichever is less

AVX

5

Bypass Network Design Procedure

1. Start at the load and work out
2. At each stage, i
   1. Size the capacitance to handle the HF current $C_i > kit/\Delta V$
   2. Size the capacitor as big as possible (economically) while keeping the inductance L_i small enough for the transient limit of the previous stage (i-1)
3. Done when capacitance is greater than $L_s(I/\Delta V)$

Really picking capacitors based on their inductance

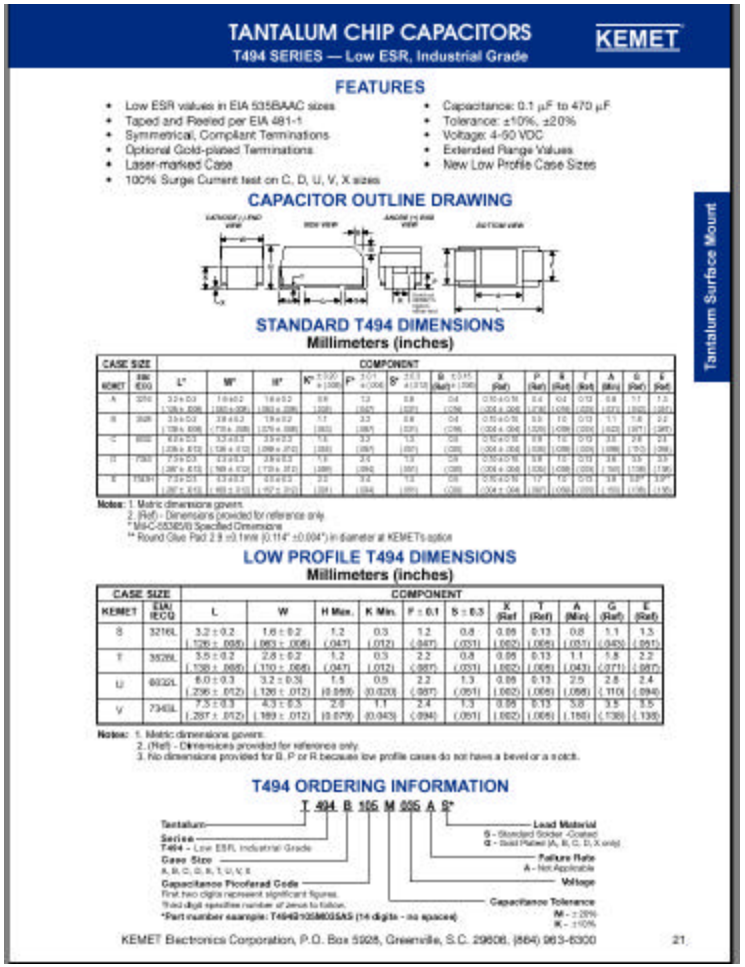
Example Design

- One chip, 10A, t_{ck} = 2ns, k = 0.5, ΔV = 0.1V, di/dt = 40A/0.5ns = 80GA/s, L_s = 100nH
- First rank
  - C1 > (0.5 x 10 x 2n)/0.1 = 100nF
  - L1 < ΔV/di/dt = 0.1/80G = 1.25pH
  - Choose on-chip 250nF capacitor
    - Could get by with 100nF, but 250nF makes the next level easier
- Second Rank
  - L2 < C1(ΔV/I)^2 = 250n(0.1/10)^2 = 0.025nH
    - First rank increases inductance limit by 20x (would have been 8x with 100nF)
  - Choose 10 2.2µF IDC caps (175pH each) on package
    - And lots (100s) of solder balls to keep total L less than 25pH

Example Design (cont)

- Third Rank
  - $L3 < C2(\Delta V/I)^2 = 22\mu\ (0.1/10)^2 = 2.2nH$
  - Choose 5 1000μF Ultra low ESR Tantalum capacitors
    - ESR of 0.018Ω each, 0.0036Ω total.
    - Current rating of 2.1A – 10.5A total
    - .036V ripple with 10A current
  - We're done since $C3 = 5000\mu F > L_s(I/\Delta V)^2 = 100n \times (10/.1)^2 = 1000\mu F$

A Typical Tantalum



TANTALUM CHIP CAPACITORS
T494 SERIES — Low ESR, Industrial Grade
KEMET

Tantalum Surface Mount

FEATURES

- Low ESR values in EIA 535BAAC sizes
- Taped and Reeled per EIA 481-1
- Symmetrical, Compliant Terminations
- Optional Gold-plated Terminations
- Laser-marked Case
- 100% Surge Current test on C, D, U, V, X sizes
- Capacitance: 0.1 µF to 470 µF
- Tolerance: ±10%, ±20%
- Voltage: 4-50 VDC
- Extended Range Values
- New Low Profile Case Sizes

CAPACITOR OUTLINE DRAWING

STANDARD T494 DIMENSIONS
Millimeters (inches)

CASE SIZE KEMET	CASE SIZE EIA/IECQ	COMPONENT L*	W*	H*	K* ±0.20 (±.008)	F* ±0.1 (±.004)	S* ±0.1 (±.004)	B ±0.15 (Ref) (±.006)	X (Ref)	P (Ref)	R (Ref)	T (Ref)	A (Min)	G (Ref)	E (Ref)
A	3216	3.2 ± 0.2 (.126 ± .008)	1.6 ± 0.2 (.063 ± .008)	1.6 ± 0.2 (.063 ± .008)	0.8 (.031)	1.2 (.047)	0.8 (.031)	0.4 (.016)	0.15 ± 0.15 (.004 ± .006)	0.4 (.016)	0.2 (.008)	0.13 (.005)	0.8 (.031)	1.1 (.043)	1.3 (.051)
B	3528	3.5 ± 0.2 (.138 ± .008)	2.8 ± 0.2 (.110 ± .008)	1.9 ± 0.2 (.075 ± .008)	1.1 (.043)	2.2 (.087)	0.8 (.031)	0.4 (.016)	0.15 ± 0.15 (.004 ± .006)	0.5 (.020)	1.0 (.039)	0.13 (.005)	1.1 (.043)	1.8 (.071)	2.2 (.087)
C	6032	6.0 ± 0.3 (.236 ± .012)	3.2 ± 0.3 (.126 ± .012)	2.5 ± 0.3 (.098 ± .012)	1.3 (.051)	2.2 (.087)	1.3 (.051)	0.8 (.031)	0.15 ± 0.15 (.004 ± .006)	0.8 (.031)	1.0 (.039)	0.13 (.005)	2.8 (.110)	2.8 (.110)	2.2 (.087)
D	7343	7.3 ± 0.3 (.287 ± .012)	4.3 ± 0.3 (.169 ± .012)	2.8 ± 0.3 (.110 ± .012)	1.3 (.051)	2.4 (.094)	1.3 (.051)	0.8 (.031)	0.15 ± 0.15 (.004 ± .006)	0.8 (.031)	1.0 (.039)	0.13 (.005)	3.8 (.150)	3.5 (.138)	3.5 (.138)
E	7343H	7.3 ± 0.3 (.287 ± .012)	4.3 ± 0.3 (.169 ± .012)	4.1 ± 0.3 (.162 ± .012)	2.2 (.087)	2.4 (.094)	1.3 (.051)	0.8 (.031)	0.15 ± 0.15 (.004 ± .006)	1.7 (.067)	1.0 (.039)	0.13 (.005)	3.8 (.150)	3.5* (.138)	3.5* (.138)

Notes: 1. Metric dimensions govern.
2. (Ref) - Dimensions provided for reference only.
* MIL-C-55365/8 Specified Dimensions
** Round Glue Pad 2.9 ±0.1mm (0.114" ±0.004") in diameter at KEMET's option

LOW PROFILE T494 DIMENSIONS
Millimeters (inches)

CASE SIZE KEMET	EIA/IECQ	COMPONENT L	W	H Max.	K Min.	F ± 0.1	S ± 0.3	X (Ref)	T (Ref)	A (Min)	G (Ref)	E (Ref)
S	3216L	3.2 ± 0.2 (.126 ± .008)	1.6 ± 0.2 (.063 ± .008)	1.2 (.047)	0.3 (.012)	1.2 (.047)	0.8 (.031)	0.05 (.002)	0.13 (.005)	0.8 (.031)	1.1 (.043)	1.3 (.051)
T	3528L	3.5 ± 0.2 (.138 ± .008)	2.8 ± 0.2 (.110 ± .008)	1.2 (.047)	0.3 (.012)	2.2 (.087)	0.8 (.031)	0.05 (.002)	0.13 (.005)	1.1 (.043)	1.8 (.071)	2.2 (.087)
U	6032L	6.0 ± 0.3 (.236 ± .012)	3.2 ± 0.3 (.126 ± .012)	1.9 (0.075)	0.5 (0.020)	2.2 (.087)	1.3 (.051)	0.05 (.002)	0.13 (.005)	2.5 (.098)	2.8 (.110)	2.4 (.094)
V	7343L	7.3 ± 0.3 (.287 ± .012)	4.3 ± 0.3 (.169 ± .012)	2.8 (0.075)	1.1 (0.043)	2.4 (.094)	1.3 (.051)	0.05 (.002)	0.13 (.005)	3.8 (.150)	3.5 (.138)	3.5 (.138)

Notes: 1. Metric dimensions govern.
2. (Ref) - Dimensions provided for reference only.
3. No dimensions provided for B, P or R because low profile cases do not have a bevel or a notch.

T494 ORDERING INFORMATION

T 494 B 105 M 035 A S*

- Tantalum
- Series: T494 - Low ESR, Industrial Grade
- Case Size: A, B, C, D, R, T, U, V, X
- Capacitance Picofarad Code: First two digits represent significant figures. Third digit specifies number of zeros to follow.
- Capacitance Tolerance: M - ±20%, K - ±10%
- Voltage
- Failure Rate: A - Not Applicable
- Lead Material: S - Standard Solder -Coated; G - Gold Plated (A, B, C, D, X only)

*Part number example: T494B105M035AS (14 digits - no spaces)

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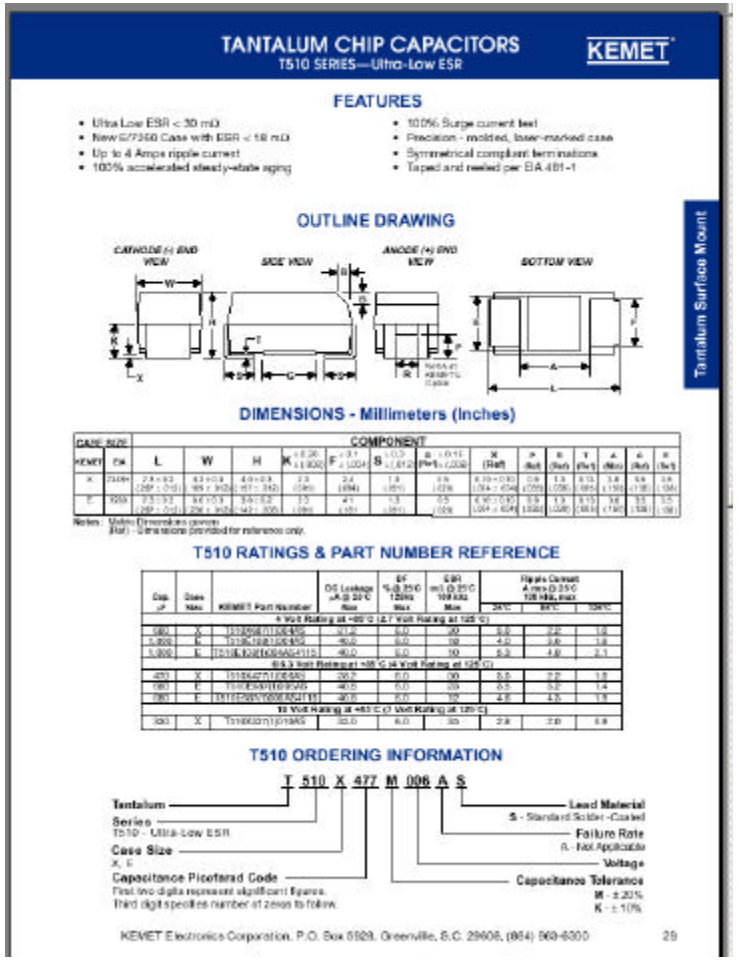

TANTALUM CHIP CAPACITORS
T510 SERIES—Ultra-Low ESR
KEMET

Tantalum Surface Mount

FEATURES

- Ultra Low ESR < 30 mΩ
- New E/7360 Case with ESR < 18 mΩ
- Up to 4 Amps ripple current
- 100% accelerated steady-state aging
- 100% Surge current test
- Precision - molded, laser-marked case
- Symmetrical compliant terminations
- Taped and reeled per EIA 481-1

OUTLINE DRAWING

DIMENSIONS - Millimeters (Inches)

CASE SIZE KEMET	EIA	COMPONENT L	W	H	K ±0.20 (±.008)	F ±0.1 (±.004)	S ±0.3 (±.012)	B ±0.15 (Ref) (±.006)	X (Ref)	P (Ref)	R (Ref)	T (Ref)	A (Min)	G (Ref)	E (Ref)
X	7360	7.3 ± 0.3 (.287 ± .012)	6.1 ± 0.3 (.240 ± .012)	4.0 ± 0.3 (.157 ± .012)	2.2 (.087)	2.4 (.094)	1.3 (.051)	0.15 (.006)	0.15 ± 0.15 (.004 ± .006)	0.8 (.031)	1.3 (.051)	0.13 (.005)	3.8 (.150)	3.5 (.138)	3.5 (.138)
E	7260	7.3 ± 0.3 (.287 ± .012)	6.0 ± 0.3 (.236 ± .012)	3.8 ± 0.3 (.150 ± .012)	2.2 (.087)	2.4 (.094)	1.3 (.051)	0.15 (.006)	0.15 ± 0.15 (.004 ± .006)	0.8 (.031)	1.3 (.051)	0.13 (.005)	3.8 (.150)	3.5 (.138)	3.5 (.138)

Notes: Metric Dimensions govern.
(Ref) - Dimensions provided for reference only.

T510 RATINGS & PART NUMBER REFERENCE

Cap. µF	Case Size	KEMET Part Number	DC Leakage µA @ 25°C Max	DF % @ 25°C 120Hz Max	ESR mΩ @ 25°C 100 kHz Max	Ripple Current A rms @ 25°C 100 kHz, max 25°C	85°C	125°C
4 Volt Rating at +85°C (2.7 Volt Rating at 125°C)								
680	X	T510X687(1)004AS	27.2	6.0	30	5.0	2.2	1.8
1,000	E	T510E108(1)004AS	40.0	6.0	18	4.0	3.0	1.8
1,000	E	T510E108(1)004AS4115	40.0	6.0	30	5.3	4.0	2.1
6.3 Volt Rating at +85°C (4 Volt Rating at 125°C)								
470	X	T510X477(1)006AS	29.7	6.0	30	5.0	2.2	1.8
680	E	T510E687(1)006AS	40.0	6.0	20	6.5	3.2	1.4
680	E	T510E687(1)006AS4115	40.0	6.0	30	4.8	4.0	1.8
10 Volt Rating at +85°C (7 Volt Rating at 125°C)								
330	X	T510X337(1)010AS	33.0	6.0	35	2.8	2.0	0.8

T510 ORDERING INFORMATION

T 510 X 477 M 006 A S

- Tantalum
- Series: T510 - Ultra-Low ESR
- Case Size: X, E
- Capacitance Picofarad Code: First two digits represent significant figures. Third digit specifies number of zeros to follow.
- Capacitance Tolerance: M - ±20%, K - ±10%
- Voltage
- Failure Rate: A - Not Applicable
- Lead Material: S - Standard Solder -Coated

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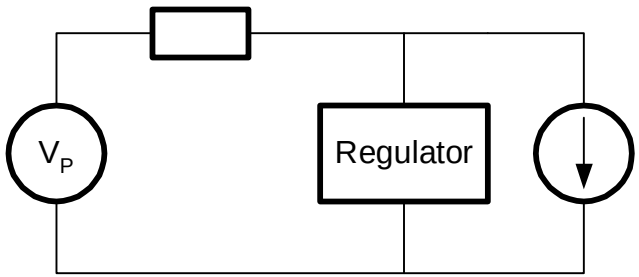
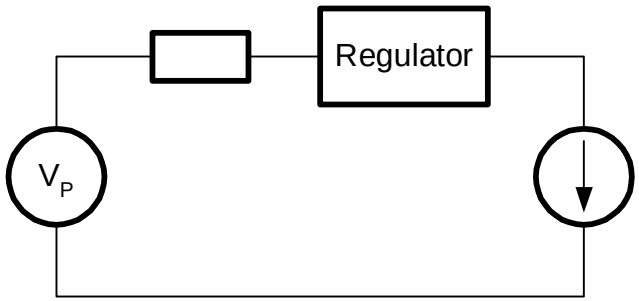
Local Power Supply Regulation

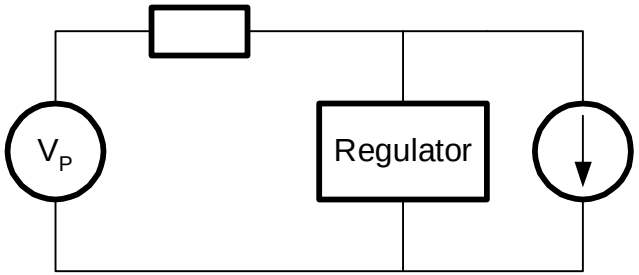
- Can put a regulator in series or parallel with the power supply
- Parallel or *shunt* regulators control current
  - add a current to the AC load current to make it look more like a DC current
- Series regulators control voltage
  - clip off the top of the voltage ripple and transient response
  - distribute power at a higher voltage (or AC voltage)





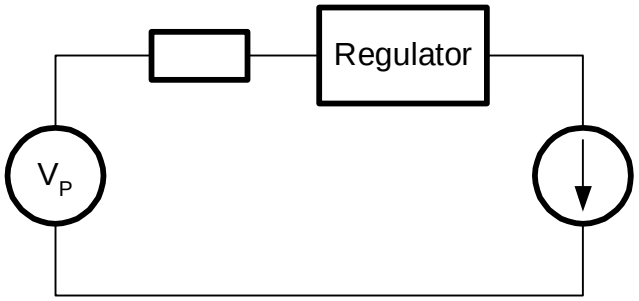
Shunt Regulators and Clamps

- Shunt regulators maintain a steady current draw from the distribution network
  - Measure the load current, I_L
  - Generate a shunt current $I_R=I_{max}-I_L$
  - Current is now DC
    - but large
- A clamp handles the turn-off transient to avoid overvoltage
  - measure the load voltage, V_C
  - draw current when V_C exceeds a threshold



Series Linear Regulators

- Think of the regulator as a variable series resistor
  - drop distribution voltage (e.g., 3.3V) down to a load voltage (e.g., 2.5V)
- Can *clip* off the top of the voltage ripple by resistively dropping it
- Limited by
  - frequency response of the regulator (can't track fast transients)
  - series nature of regulator, can't divert transient inductor current



Switching Regulators

- A *switching* regulator uses a reactive element (usually a transformer or inductor) to convert the supply from one voltage to another with only a small loss in power
- Distributing power at a high voltage improves things quadratically
  - less current to distribute
  - more voltage to tolerate ripple
- Often advantageous to make this distribution voltage AC (at 0.1kHz to 1MHz)

$$V_D = kV_P$$

$$I_D = \frac{I_P}{k}$$

$$\frac{\Delta V_D}{V_D} = \frac{Z_D I_D}{V_D} = \frac{Z_D I_P}{k^2 V_P}$$

Next Time

- On-Chip Power Distribution