EE273 Lecture 16
Wrap Up and Project Discussion

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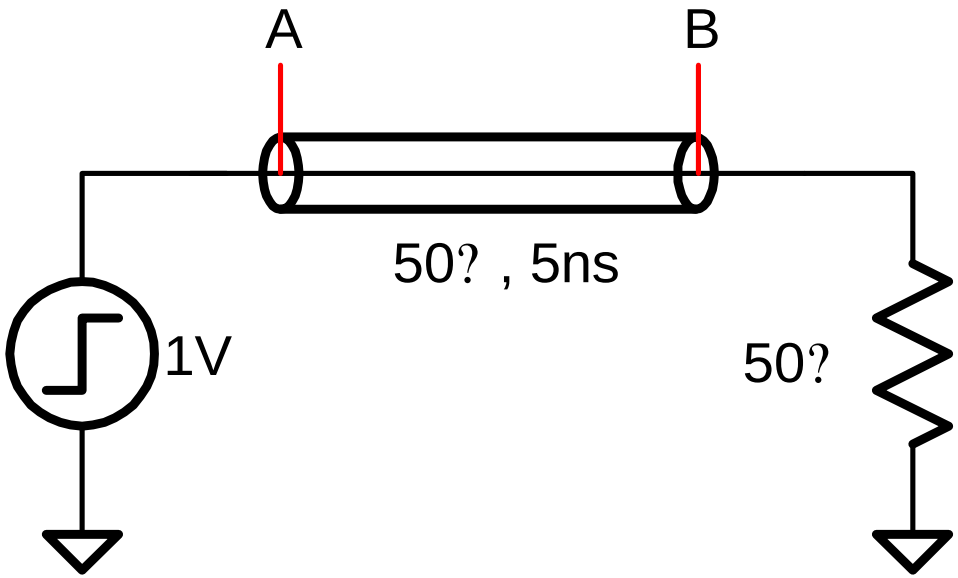
Logistics

- Final Exam
  - Friday 3/23, 8:30AM to 10:30AM
  - Location Terman Auditorium
- Upcoming Lecture Schedule
  - 3/14 – Guest lecture – Jeff Cain (Cisco)

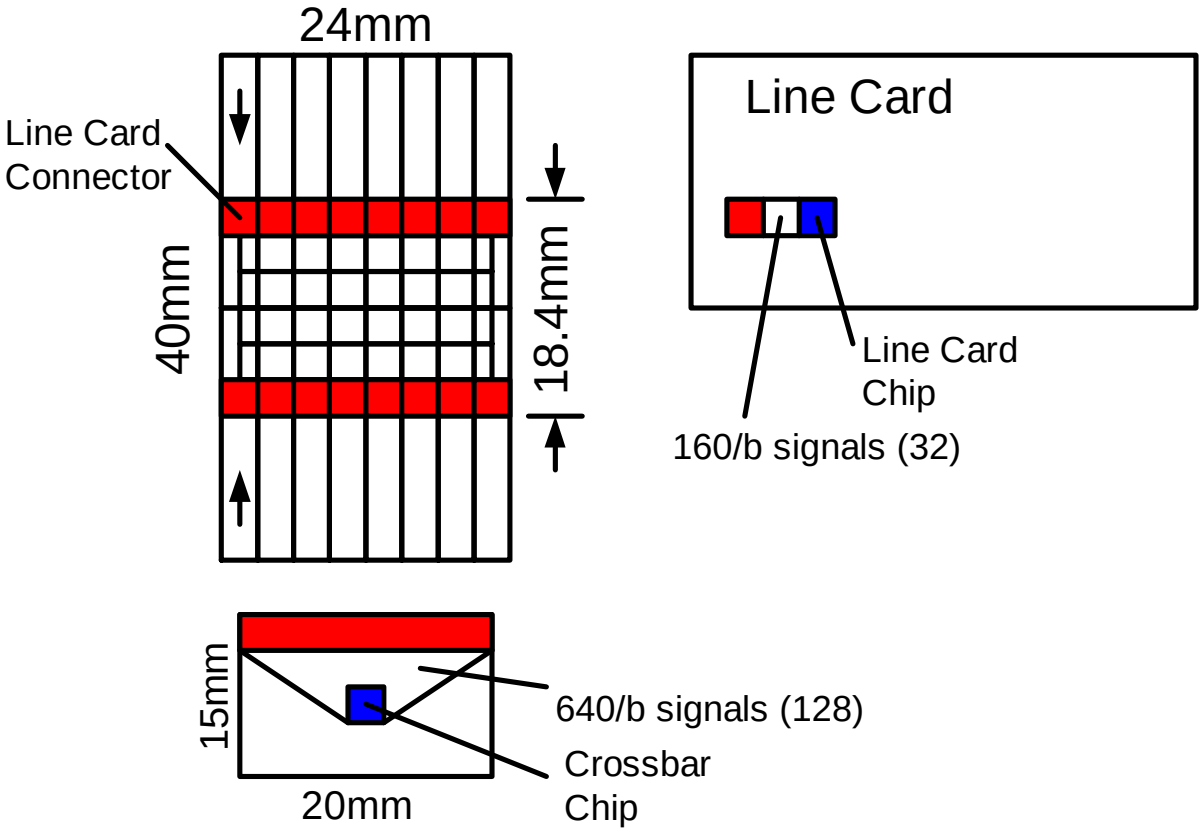
Wires

- Treat as transmission lines
  - Simple model: waves propagate, reflect, superpose
  - Second order effects: loss, discontinuities



Project View of Wires
Start with Physical Layout

Line Cards - Front Side
Crossbars - Back Side



Project view of wires (2)
Make design choices

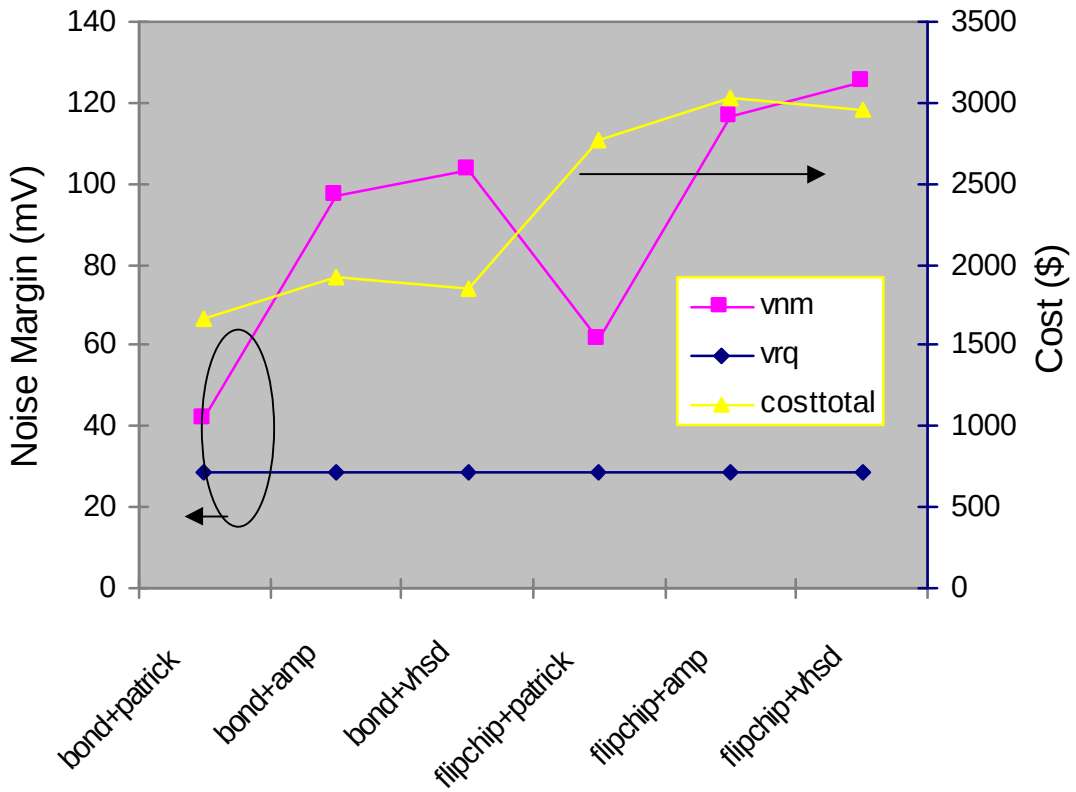
- Package
  - Wire-bond or flip-chip
- PCB
  - Material, number of layers, stackup, transmission line geometry
- Connector
  - Selection
- Trade off
  - Performance, cost, risk
  - Considerable work to collect information and evaluate tradeoffs

An Example

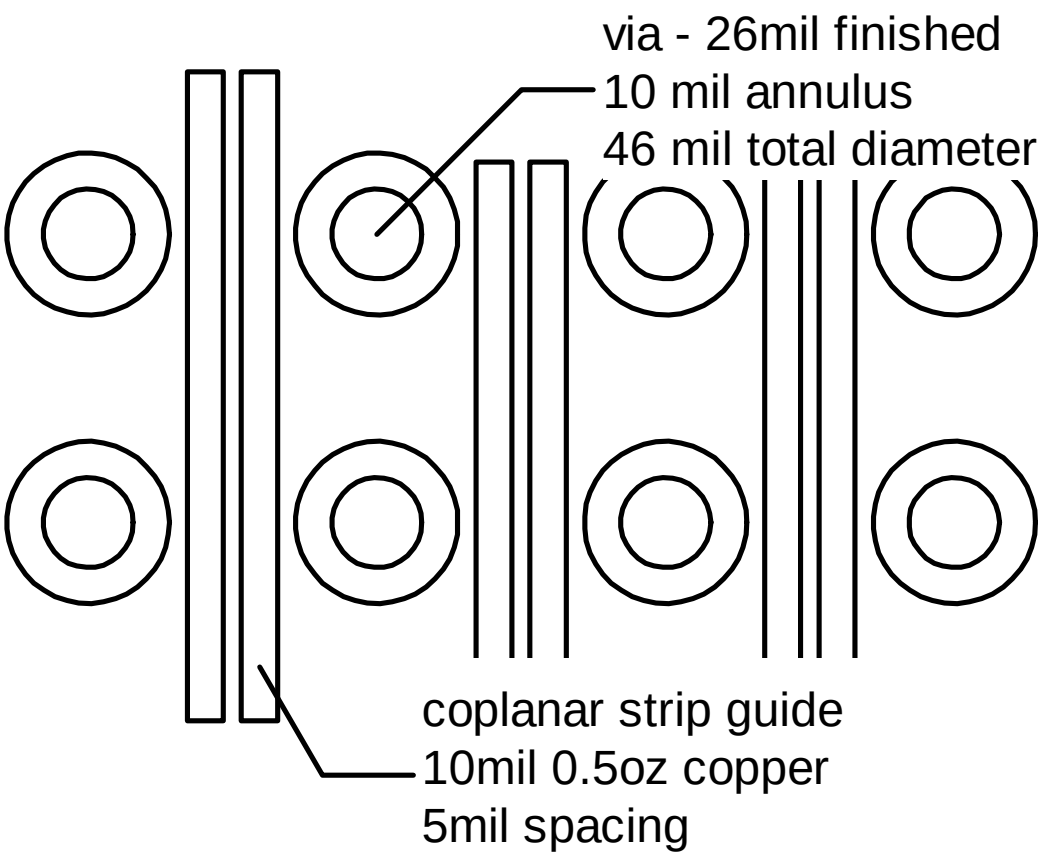
(Yohan Frans, James Hsu, Gaurav Chandra, Pawan Kapur)

Connect and package choise Analysis:
Unidirectional Signaling with 10 mA current Swing

vrq:Required Noise Margin
vnm:Attained Noise Margin



Project view of wires (3)
Negotiating a via Field

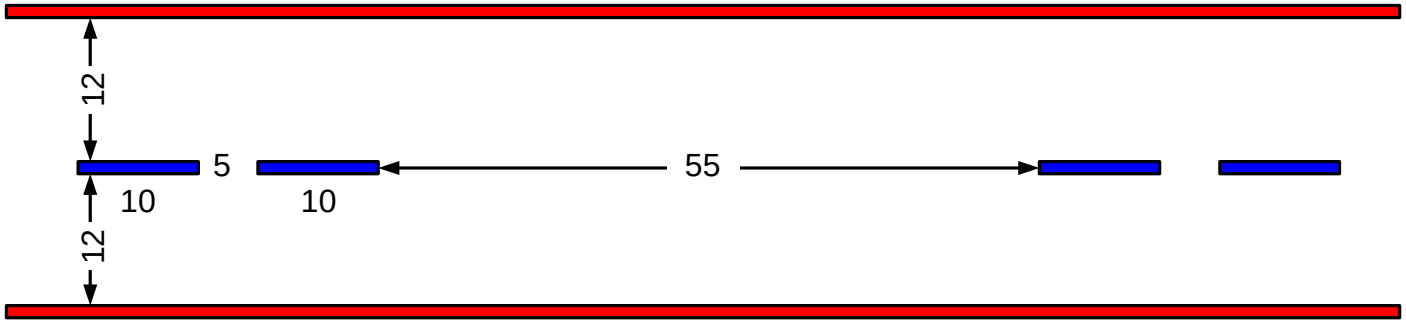


Can only fit one coplanar stripguide pair between every row of via pins per layer

At 5Gb/s, need 32 pairs from each side for each 3mm (15-rows) of backplane.

Need 5 signal layers – 11-layer backplane with ground shields

Project view of wires (4)
The Stackup

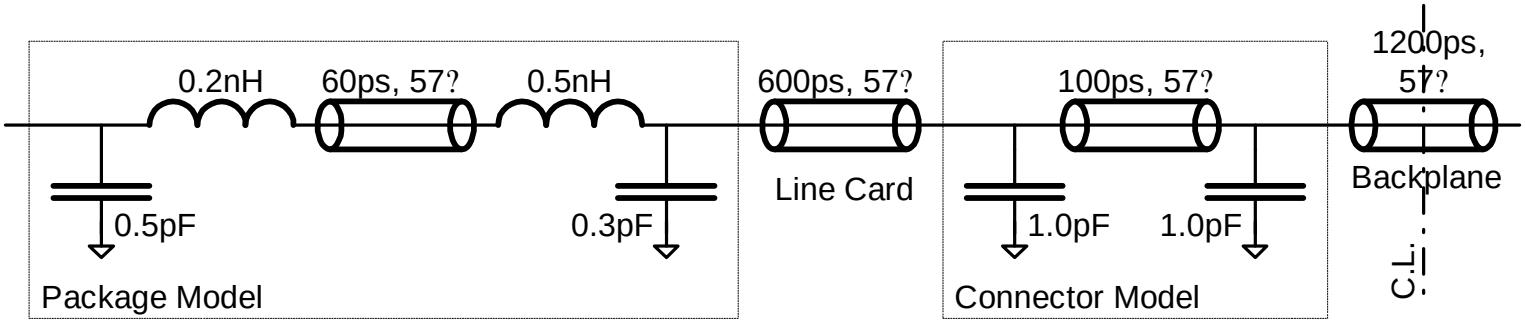


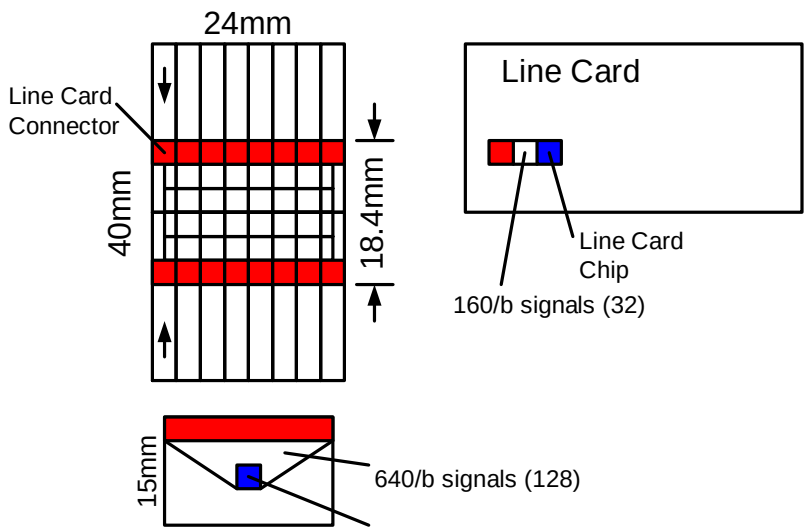
LinPar Output

```
MATRIX [L] (H/m)            MATRIX [R] (ê/m)
   3.910E-07  8.611E-08        2.447E+01  7.933E-01
   8.611E-08  3.910E-07        7.933E-01  2.447E+01

 MATRIX [C] (F/m)            MATRIX [G] (S/m)
   1.196E-10 -2.634E-11        2.302E-03 -5.069E-04
  -2.634E-11  1.196E-10       -5.069E-04  2.302E-03

  APPROXIMATE CHARACTERISTICS OF ISOLATED LINES

  LINE #   CHARACTERISTIC   WAVE VELOCITY   EFFECTIVE RELATIVE  ATTENUATION
           IMPEDANCE (ê)       (m/s)          PERMITTIVITY       (dB/m)

     1        5.717E+01       1.462E+08          4.204E+00       2.430E+00
     2        5.717E+01       1.462E+08          4.204E+00       2.430E+00
```

132mil thick backplane

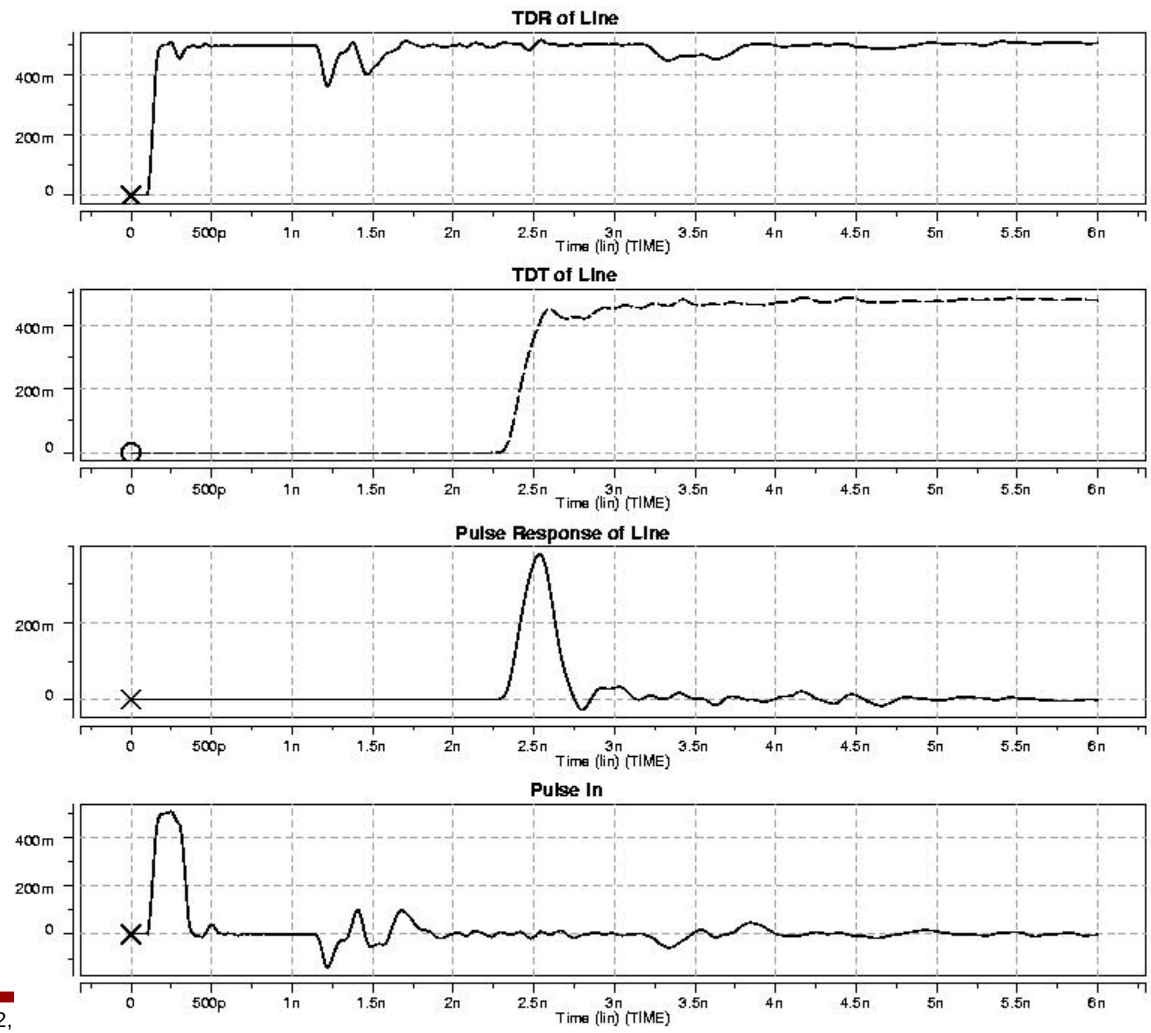
Project view of wires (5)
Develop a Model



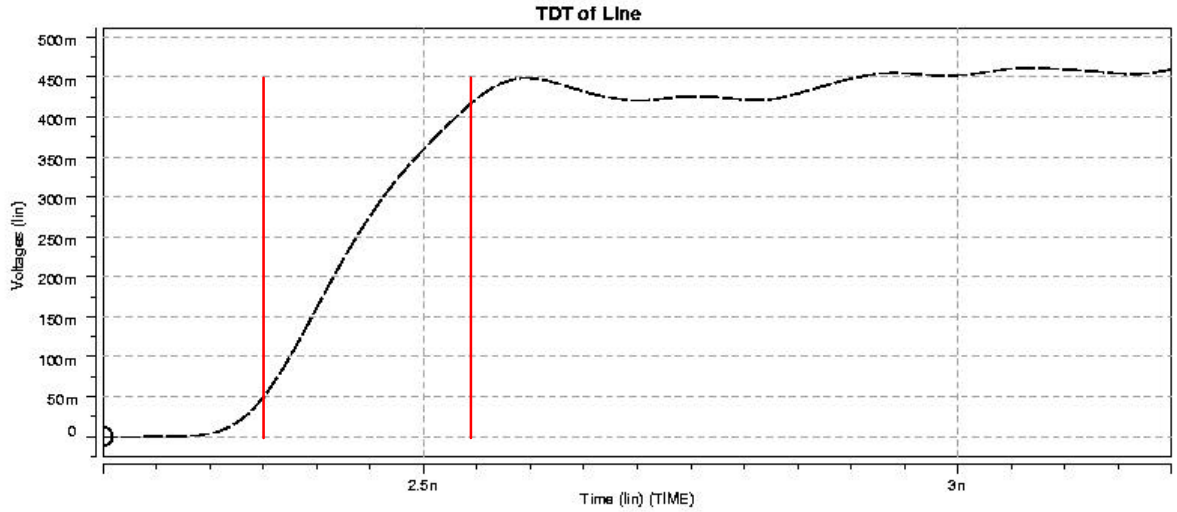


In practice, the SPICE model is validated against a prototype

Project view of wires (6)
Test the model



A Closer Look



A = 375/450 = 0.83

(17% attenuation)

ISI = 50/350+30/350

ISI = 23%

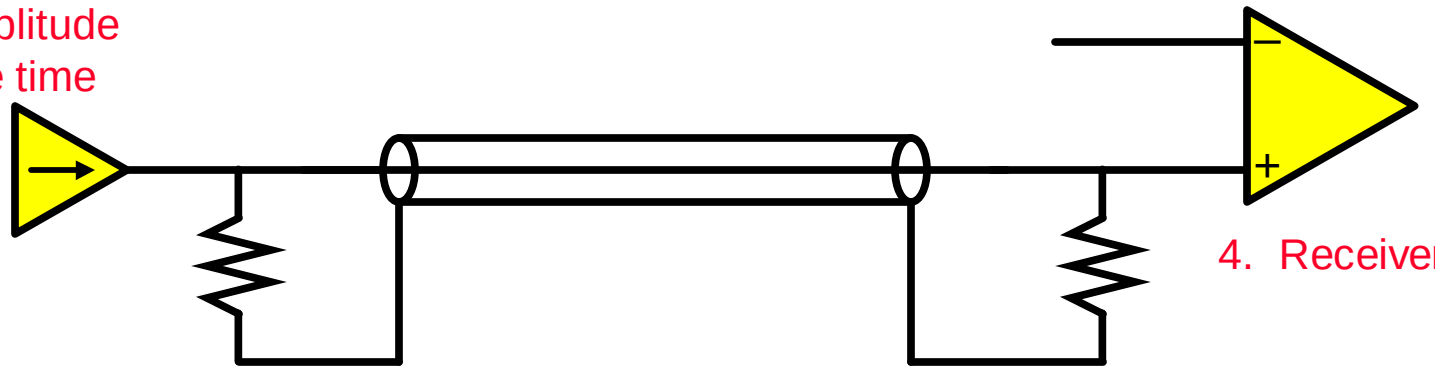
Signaling & Noise

- A good signaling system isolates the signal from noise rather than trying to overpower the noise
  - crosstalk - terminate both ends
  - ISI - matched terminations, no resonators, rise-time control
  - Power supply noise - current mode, stable reference, differential signaling
  - Reference noise - bipolar signaling, differential signaling

Elements of a Signaling System

1. Transmitter:
   output impedance
   bipolar vs. unipolar
   amplitude
   rise time

3. Reference



4. Receiver

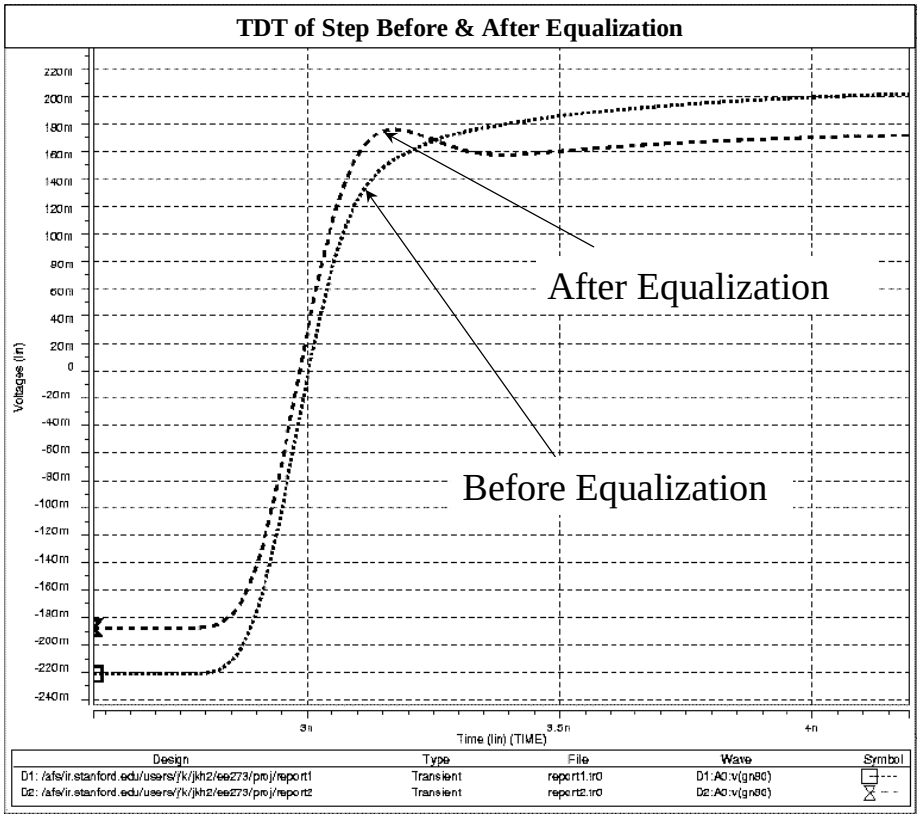
2. Termination method

2. Termination method

Project view of Signaling (1)
Design Decisions

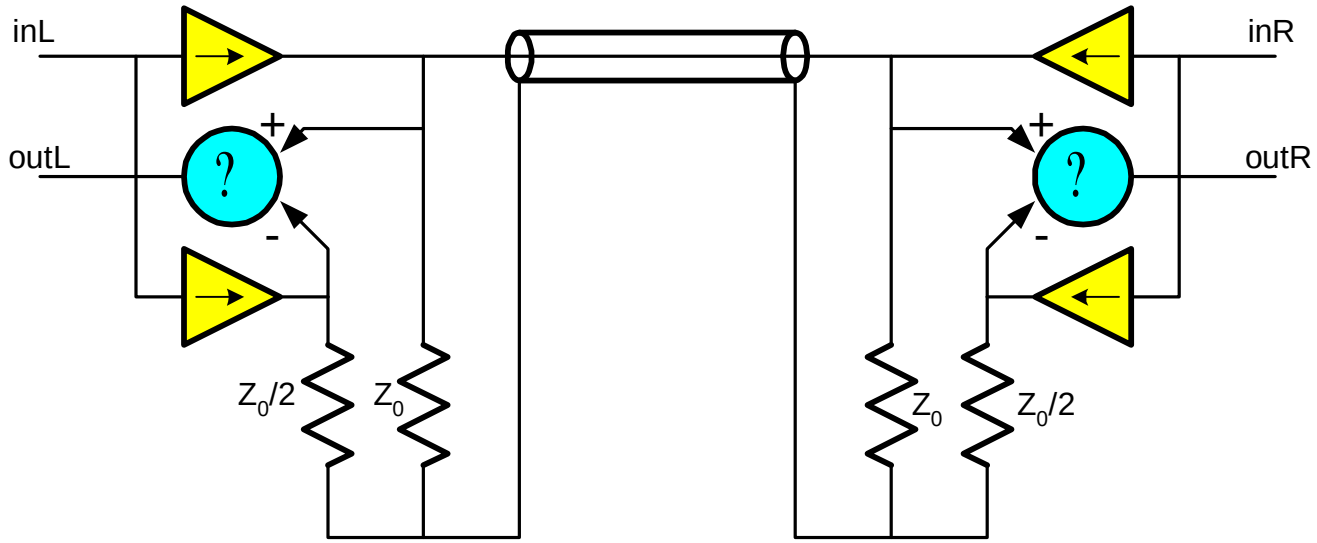
- Signaling mode (termination method)
  - Terminating both ends in a matched impedance universally used
    - Some used 20% resistors, some 5%
      - Tx levels, not reflection the major issue here
- References
  - Differential signaling provides a reference, eliminates AC return current and makes numerous noise sources common mode
- Signal levels
  - To overcome Gaussian noise of 4mV and 10+ mV of receiver offset and sensitivity generally requires about 10mA of current
    - More efficient to provide this as +/-5mA (bipolar signaling)
- Noise cancellation
  - Transmit pre-emphasis to equalize frequency-dependent attenuation
  - Additional FIR filters to cancel crosstalk, etc…

Equalization

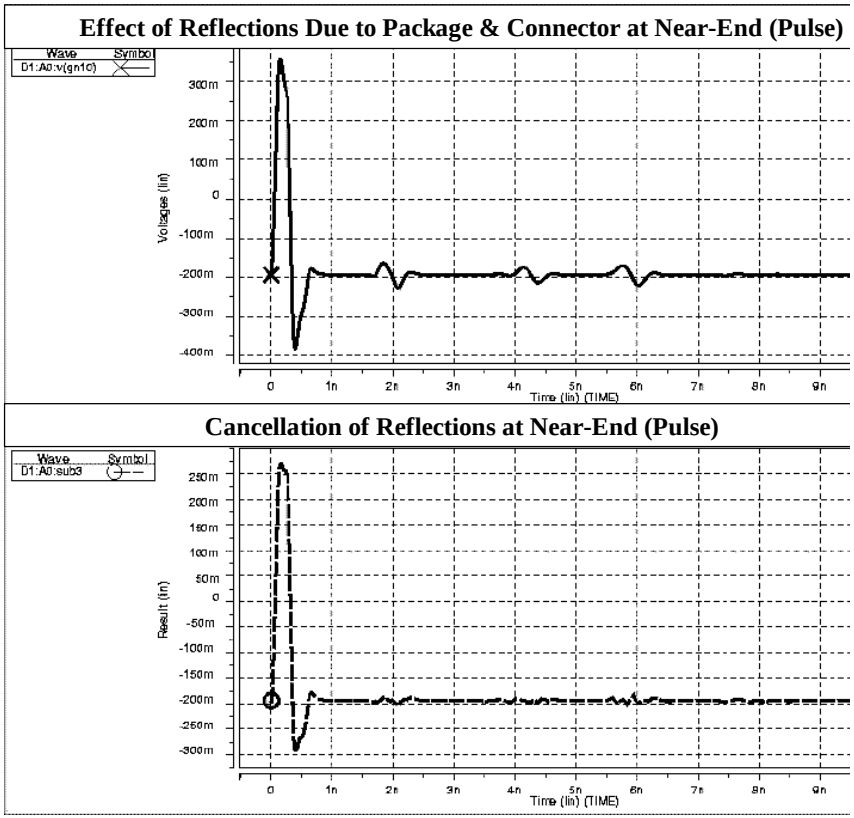


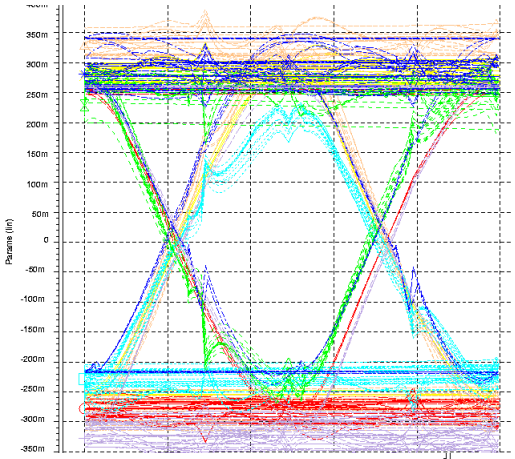
(Yohan Frans, James Hsu, Gaurav Chandra, Pawan Kapur)

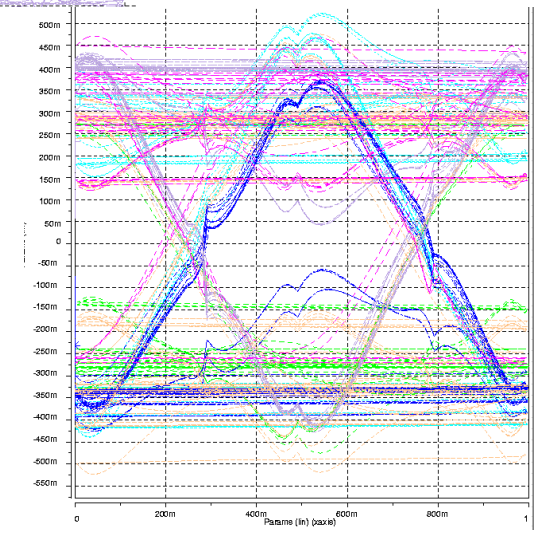
Simultaneous Bidirectional Signaling
The Circuit



Reverse-Channel Crosstalk Cancellation







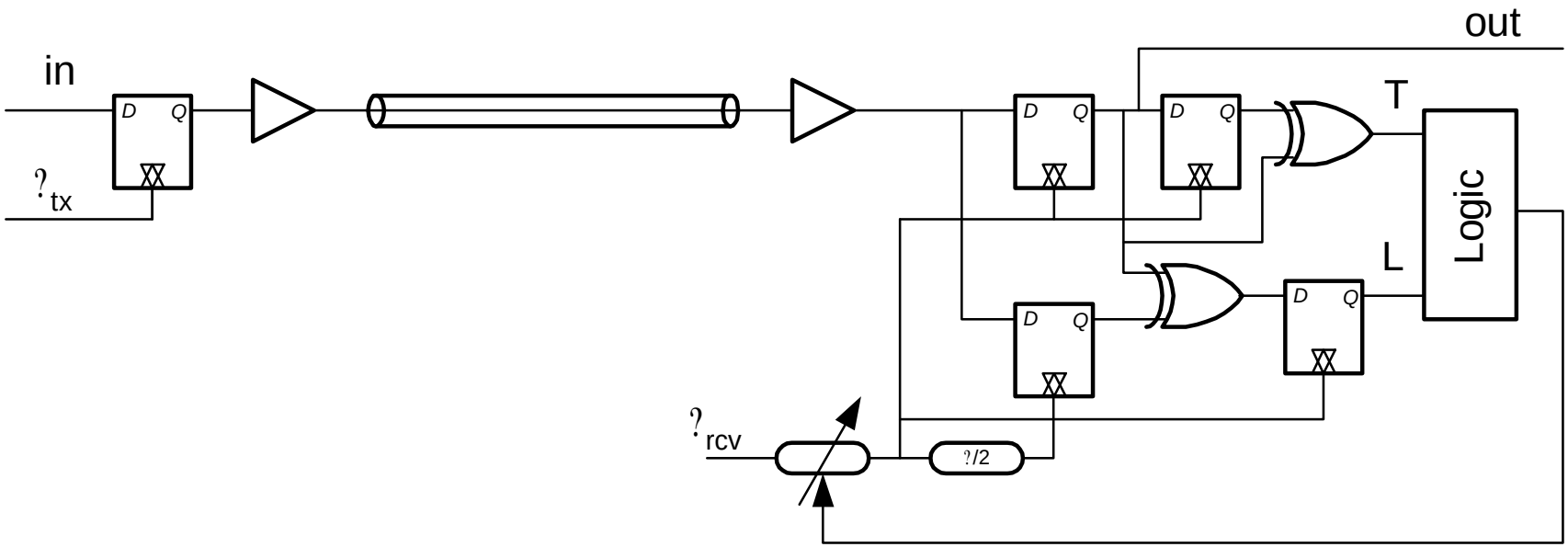
A Noise Budget

Noise Budget					
DV/2	250	mV	half differential signal swing		
Tx offset	0.05		can be 5% low		
Tx R	0.05		launch 5% low wave		
Attn	0.23				
Tx red	0.33				
VGM	167.5	mV	at receiver		
ISI	0.23		after equalization (from SPICE)		
Xtalk	0.1		from connector		
KN	0.33				
VKN	110.55	mv	proportional noise		
VRx	15	mV	offset and sensitivity		
VNM	41.95	mV			
VG	4	mV			
VSNR	10.49				
BER	1.31E-24	1/s			

Timing Decisions

- Per-line closed-loop timing needed above 1Gb/s
  - Have to cancel skew
- Where do events originate
- Local clock or reference clock sent with signal bundle
  - 1 extra pair makes some jitter common mode
  - Timing dominated by jitter of local PLLs
    - 10% at each end vs. 10% total
- Some timing noise is proportional, some isn't
  - Timing circuit jitter decreases with frequency
  - Data-dependent jitter increases
  - Rise-time determined by media
  - Aperture time fixed

Link with per-line Closed-Loop Timing



If a reference clock is sent, it can be shared over the entire bundle

Project as a Whole

- Realistic depiction of how a subset of digital systems engineering principles are applied in practice.
- Highlights ‘engineering method’
  - Sketch a design
  - Create a model
  - Use model to tradeoff design alternatives
  - Get data from vendors to incorporate into model
  - Refine design
  - Analyze to validate that objectives are met

Next Time

- Guest Lecture by Jeff Cain of Cisco