INTERCONNECT APPLICATION NOTE

tyco / Electronics

AMP Z-PACK HS3 Connector Routing

Report # 20GC004-1

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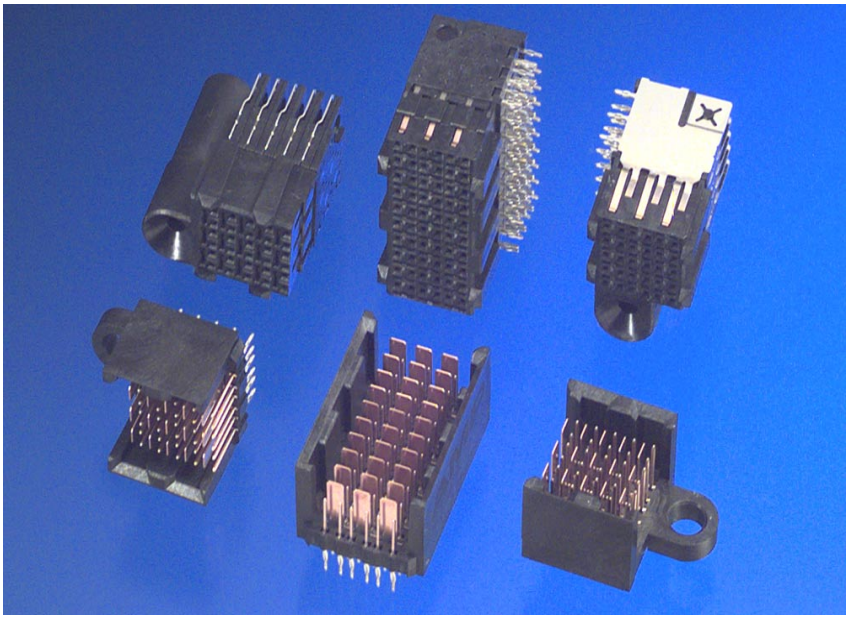

Z-PACK HS3 6 Row 60 Position and 30 Position Connectors

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AMP Z-PACK HS3 Connector Routing

I. Introduction

As engineers design systems that attempt to push serial speeds across backplane environments in the gigabit per second range, the selection of the system's electrical connector becomes more significant. Electrical, mechanical, and manufacturing aspects of the connector must be considered simultaneously. At the board level these aspects combine with common board design practices to influence the design of the connector-to-board interface and how the board itself will be routed. The manner in which the connector is designed into the system can significantly impact the system's intended performance.

Tyco Electronics has been actively researching these areas in an effort to help customers use the Z-PACK HS3 connector in gigabit serial systems. The combination of interconnect research and intimate knowledge of the connector is presented to provide insight into the capability of an Z-PACK HS3-based system design. Furthermore, this document provides specific design recommendations that will address layout, electrical performance, and manufacturability tradeoffs of the connector at the board level.

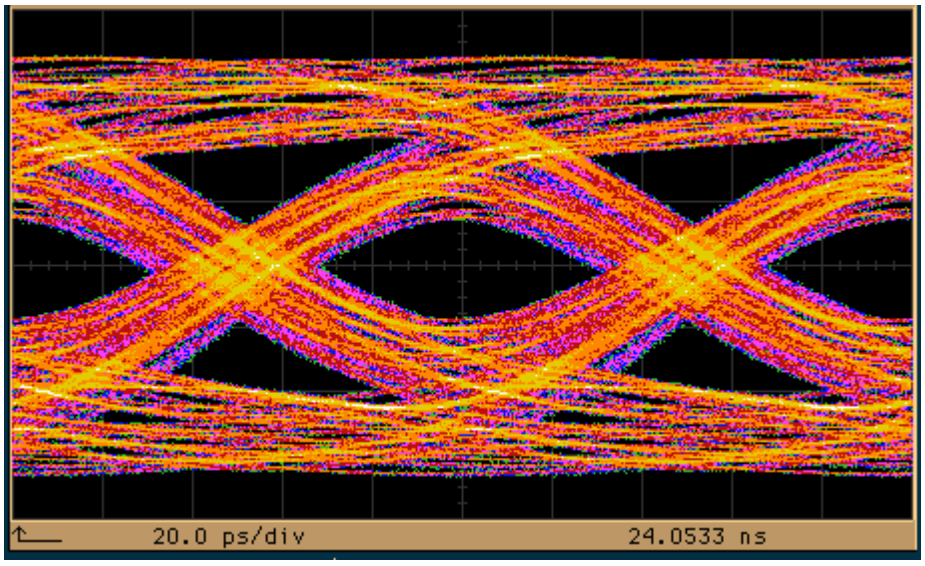


Figure 1: AMP Z-PACK HS3 connector operating in a 10 Gbps serial system environment

II. Connector Overview - Z-PACK HS3

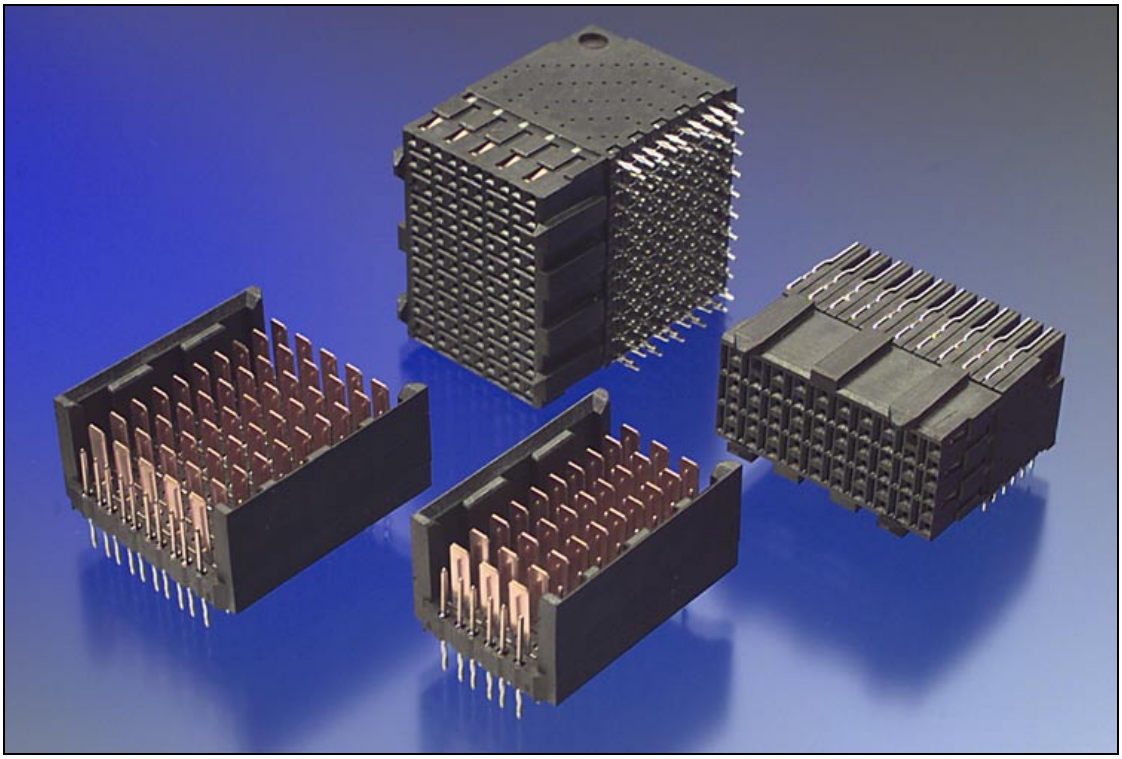


Figure 2: Z-PACK HS3 10 Row (100 position) and 6 Row (60 position) Connectors

The AMP Z-PACK HS3 connector shown in *Figure 2* has been developed for high-speed signal applications and is targeted for systems with high signal density or noise-sensitive signals. These applications work well with the Z-PACK HS3 due to ground shields that are placed between pin columns. The ground shields nearly eliminate noise between connector columns, allowing the use of higher signal densities while maintaining signal impedances of 50 Ω single-ended and 100 Ω differential.

Two different pin count versions of the Z-PACK HS3 connector are available for both 10 row and 6 row connectors. These two versions are a 10 column version (100 or 60 position) and a 5 column version (50 or 30 position). The 5 column version is available with an optional multi-purpose alignment region for coding keys and a guide pin. Also, the Z-PACK HS3 is available in right-, center, and left-handed versions. The difference between these versions is the orientation of the guide pin and coding key regions. All modules use press-fit pin technology and employ dual beam receptacles.

Part numbers for each connector module are provided in Figure 3 and Figure 4. Further product information can be found in AMP catalog #1307515 and the Z-PACK HS3 specific subset, catalog #1307397.

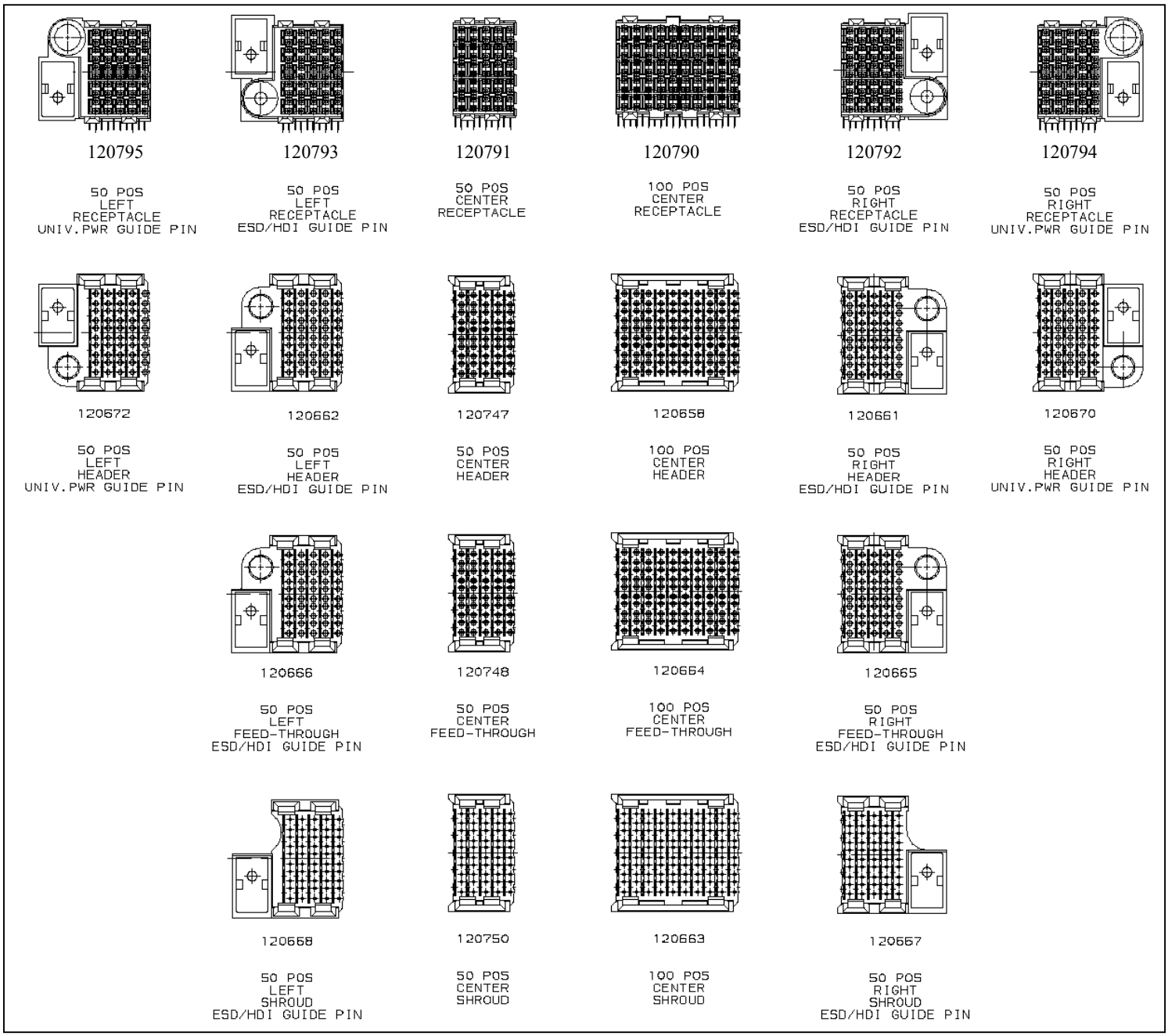


Figure 3: 10 Row Product Family

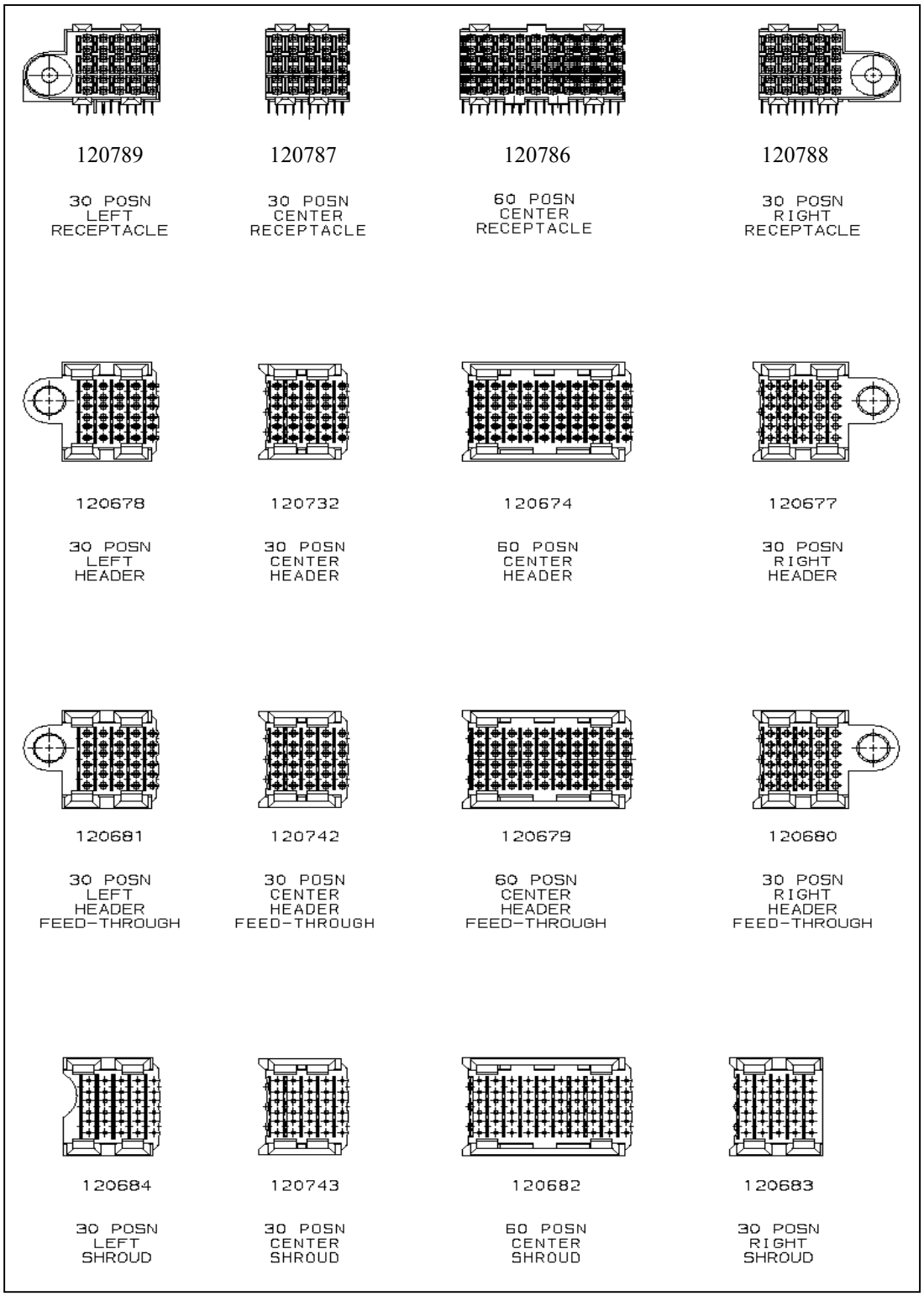


Figure 4: 6 Row Product Family

III. Connector Footprint

A. Dimensions

Full mechanical dimensioning and tolerances are available for all versions of the Z-PACK HS3 connector. See section VII for details. The dimensions critical to routing of the Z-PACK HS3 connector are related to the hole pattern, or "footprint", of the connector as shown in Figure 5. All dimensions within the footprint are identical for both the backplane (header) and daughter card (receptacle) components. Both signal and ground pins have identical hole sizes. Figure 5 and Table 1 below are provided to quickly identify critical hole dimensions for the circuit board. Manufacturing dependant dimensions are discussed later in this document.

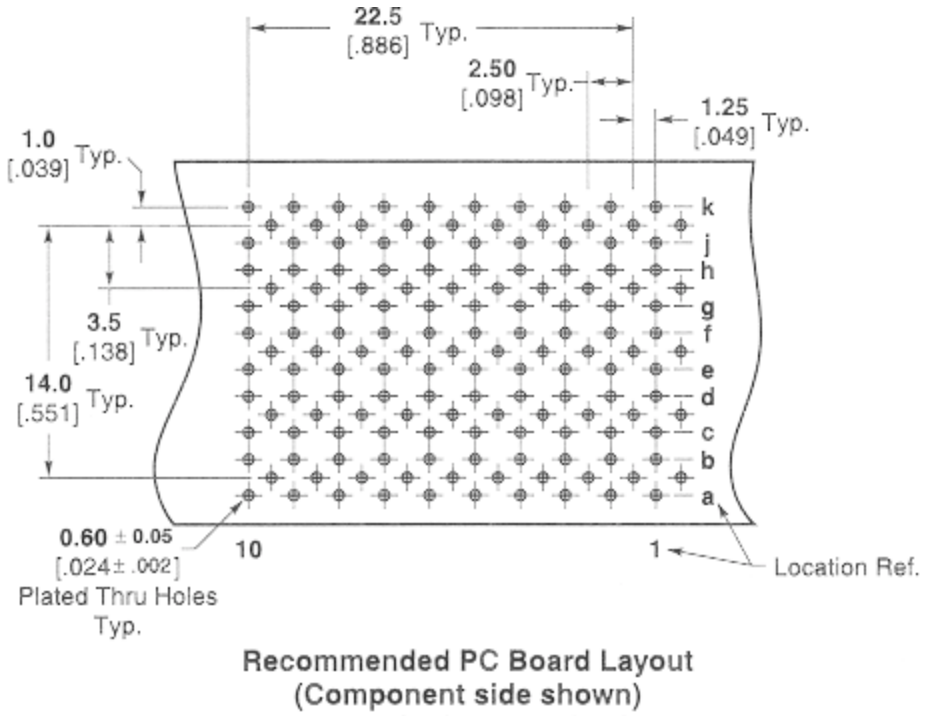


Figure 5: Footprint Dimensions (10 row 10 column module)

Hole Dimension	**Diameter mm (in.)**
Drill Hole Size	0.70 ± 0.025 (0.0276 ± 0.001)
Finished Hole Size	0.60 ± 0.05 (0.024 ± 0.002)
Copper Thickness of Hole	0.0375 ± 0.0125 (0.0015 ± 0.0005)

Table 1: Connector Hole Dimensions

B. Fabrication Technology

Other important dimensions for board layout are determined by the capabilities of the circuit board fabricator. Current high-tech PCB industry fabrication technology (i.e. capability) requires minimum pad sizes ranging from D+10 mils through D+18 mils, where "D" is the diameter of the drilled hole size (1 mil is 0.0254 mm (0.001")). For the Z-PACK HS3 connector this results in minimum pad sizes ranging from 0.96 mm (0.038") to 1.16 mm (0.046"). These resultant pads are the minimum pad sizes required to maintain 0.05 mm (0.002") of annular ring for a given PCB manufacturer's capability. Annular ring is an industry standard measure of the clearance between the pad edge and worst case drill edge after manufacturing. Because the Z-PACK HS3 is typically used in high speed or dense applications where routing issues are most significant, *all pad dimensions in this document will assume a D+12 mil pad size, or 1.02 mm (0.040") pad, unless otherwise specified*. The pad diameter may be optimized for specific project needs, and should be evaluated on a project and vendor basis. Designing with a D+10 mil technology PCB could mean reduced yields or breakout, potentially adding cost to the PCB or violating industry specification compliance.

Note: A minimum pad to trace clearance of 0.13 mm (0.005") will also be assumed for calculating routing dimensions.

1. Pad Size

Based upon the D+12 mil fabrication technology assumption, a 1.02 mm (0.040") diameter pad should be used with all Z-PACK HS3 connector pins. For very high-tech PCBs (D+10 mil) the pad is 0.97 mm (0.038"). In some cases the reduced manufacturability of a D+10 mil technology PCB is required to reduce pad sizes, although potentially reduced yields or breakout may add cost to the PCB. Where possible the largest appropriate pad size should be used to provide the PCB manufacturer with the greatest flexibility, thereby reducing overall system costs.

Thermal reliefs are not required on ground or power pins, because the Z-PACK HS3 connector uses a press-fit technology. A direct connection to reference and power planes will offer the lowest inductance connection to the circuit board.

2. Antipad Size

Antipads, or plane clearances (Figure 6), are required to separate signal holes from reference voltages to avoid shorting. Choosing the proper size of these clearances is critical in determining several other design parameters: signal integrity, EMI, voltage breakdown, and manufacturability. The antipad for the Z-PACK HS3 is limited to a minimum of 1.27 mm (0.050") due to manufacturability and a maximum of 1.60 mm (0.063") by signal integrity. A minimum antipad should be at least 0.25 mm (0.010") in diameter larger than it associated pad.

Determining the proper antipad size within the 1.27 mm (0.050") to 1.60 mm (0.063") range depends upon system design goals.

Antipad sizes are minimized:

- To reduce noise by closely shielding adjacent pins with reference planes
- To reduce EMI by minimizing aperture sizes in reference planes
- To maintain a strong reference to ground for single-ended signals and ground referenced differential signals

Antipad sizes are maximized:

- To maximize voltage breakdown spacing between the pin and the reference plane
- To increase manufacturability by reducing the chance of shorting.
- To reduce reflections in a high speed gigabit serial system by reducing the capacitive effect of the plated through-hole.

A comparison of the system performance of the 1.60 mm (0.063") antipad to a smaller 1.32 mm (0.052") antipad, shown in Figure 7, demonstrates how increasing the antipad size can increase overall system performance due to minimized system reflections. The diagrams in Figure 7 show an 18" point-to-point link with two AMP Z-PACK HS3 connectors operating at 5 Gbps, as described in the DesignCon 2000 Presentation referenced in section VII.

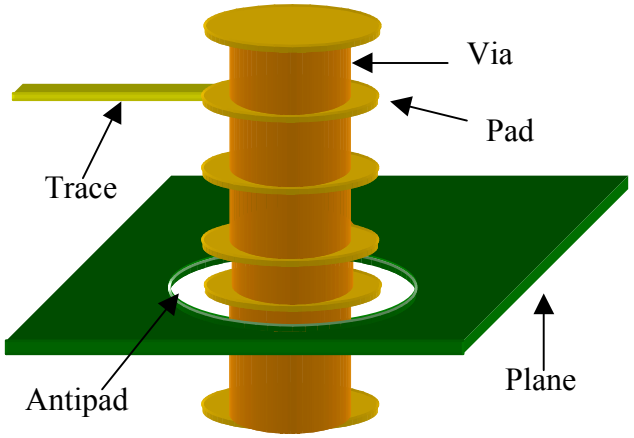


Figure 6: Trace, Via, and Antipad in Plane

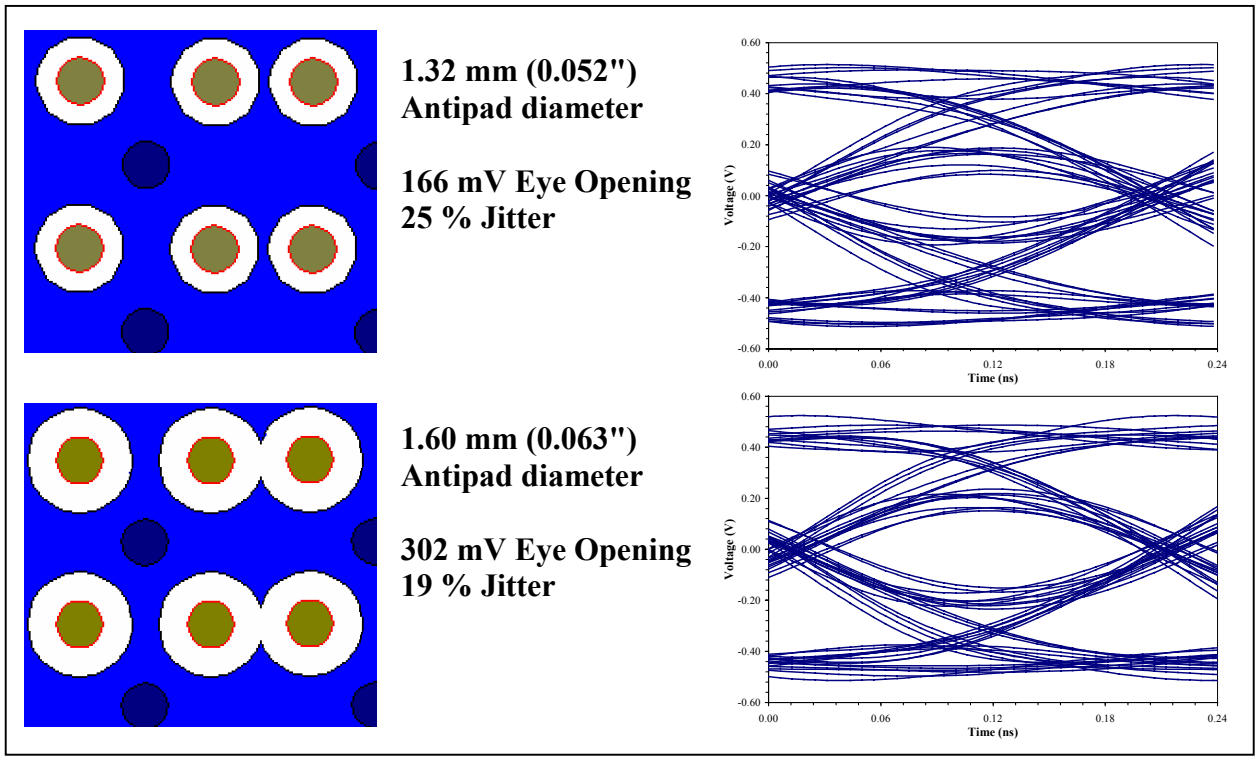


Figure 7: Antipad Performance Comparison

3. Non-functional Pads

The removal of non-functional internal pads will improve signal integrity and manufacturability of the PCB. However, some assembly facilities prefer that pads are left in order to maintain hole integrity through various soldering processes. For electrical reasons it is recommended to remove unused pads on internal layers.

IV. Routing

Because the Z-PACK HS3 connector can be used for both single-ended and differential signals, the routing of both signal types will be examined. Whether routing into or through the Z-PACK HS3 pinfield, the general guidelines are the same.

A. Routing Channels

Between each column of signal pins are two routing channels for traces. When routing edge-coupled differential signals through or into the pinfield, traces should be symmetrical around ground pins, not signal pins. Both recommended and non-recommended routing styles are shown in Figure 8. When routing differential signals around the ground pins, the traces should be kept as close to the ground pins as manufacturing will allow, in order to reduce noise if differential spacing permits. Single-ended and broadside-coupled differential signals use the same routing channels as edge-coupled differential signals but should be centered between signal and ground pins to maximize trace-to-trace isolation and reduce trace crosstalk. The Z-PACK HS3 connector also has vertical routing channels that can be utilized in the same fashion as the horizontal channels.

Recommended Differential Routing

Non-Recommended Differential Routing

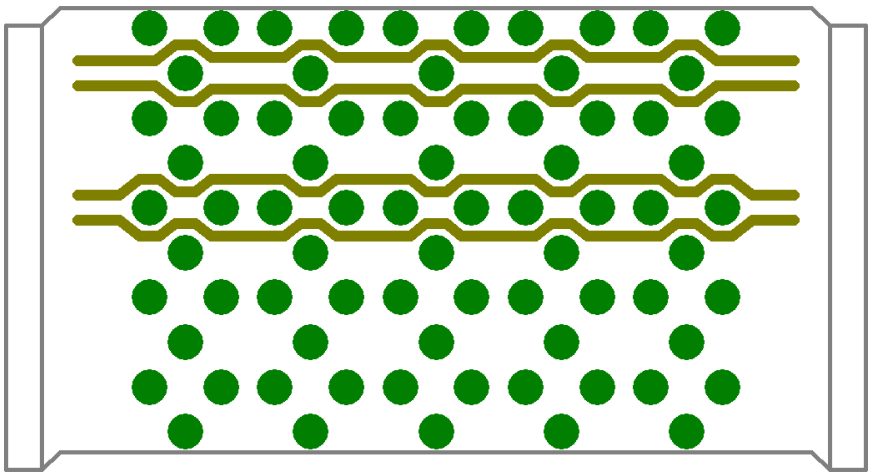


Figure 8: Routing Methods

B. Trace Widths

The narrowest area of the connector footprint is the diagonal routing between a signal pin and a ground pin. This diagonal region is labeled as "B" in Figure 9 and is applicable to both the header and receptacle parts. At location "B", there is a 0.56 mm (0.022") space between 1.02 mm (0.040") pads. This allows for a maximum of a 0.30 mm (0.012") wide trace ("A") to be routed in the diagonal region, assuming that a trace to pad spacing of 0.13 mm (0.005") is required. If the trace is routed off-angle (not 45°), then an additional 0.0254 mm (.001") in trace width or spacing can be gained beyond 0.30 mm (0.012").

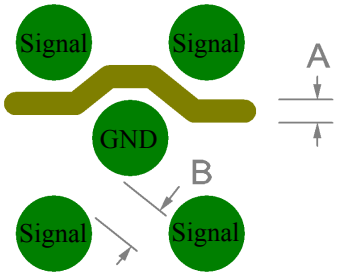


Figure 9: Footprint Dimensions

C. Quad Track Routing

Typically two traces are routed between signal columns in the Z-PACK HS3 connector due to the 0.56 mm (0.022") dimension between a signal and ground pin in the footprint. If manufacturing constraints (either D+12 mil or pad-to-trace spacing) are relaxed by .076 mm (.003") then four narrow traces can be routed between signal columns where previously two traces fit. Antipad sizes must also be minimized to maintain ground coverage for the additional traces. Quad track routing (4 traces or 2 differential pair between signal columns) should only be used for low speed, high density designs that can accommodate the additional trace crosstalk and attenuation. System level noise analysis should be performed when the Z-PACK HS3 connector is used in this fashion to determine the performance effects. Additionally, this would reduce the number of layers required to route out of the connector by half. Both routing methods are shown below in Figure 10.

Dual Track Routing

Quad Track Routing

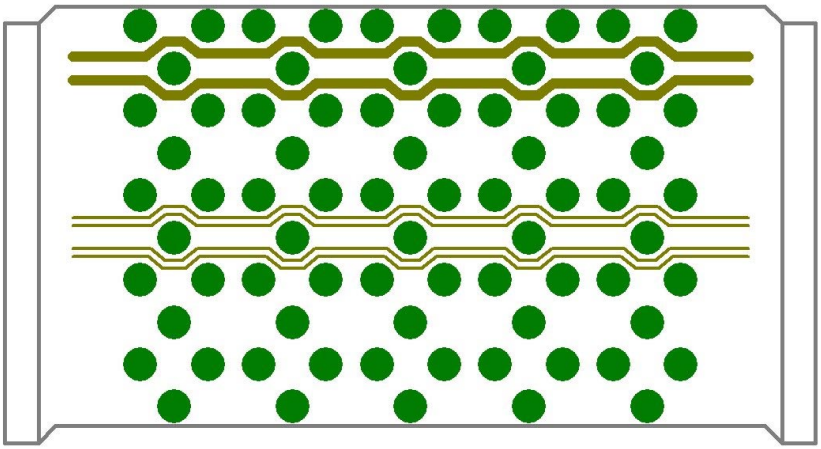


Figure 10: Example of Dual and Quad Track Routing of the Z-PACK HS3 Footprint

D. Connector Footprint Breakout

1. Z-PACK HS3 6 Row Breakout

If routing out of both sides of the connector is possible, then only **1 signal layer** is required for the 6 row Z-PACK HS3 connector breakout on a motherboard (or backplane). Otherwise, if only one routing direction is used, the daughter card breakout example can be used which requires a minimum of **3 signal layers** (with some free remaining channels) to route out of a fully populated 6 row Z-PACK HS3 connector. For configurations where there are remaining routing channels on a layer, only half of the last routing layer is needed by the breakout pattern. Examples of typical breakout patterns for the Z-PACK HS3 6 row connector pinfields are shown in Figure 11 – Figure 13. Section VII lists available CAD tool-specific layout examples for the Z-PACK HS3 connector.

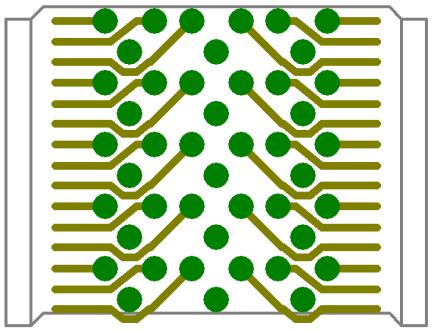


Figure 11: Backplane Single-Ended Breakout Pattern (1 Layer)

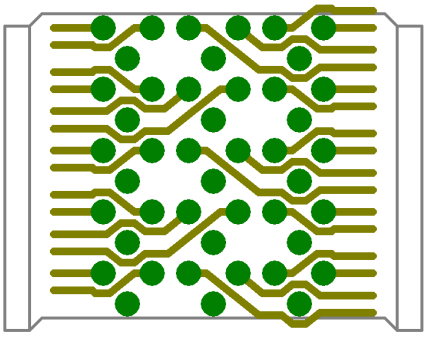


Figure 12: Backplane Differential Breakout Pattern (1 Layer)

Backplane

Daughtercard

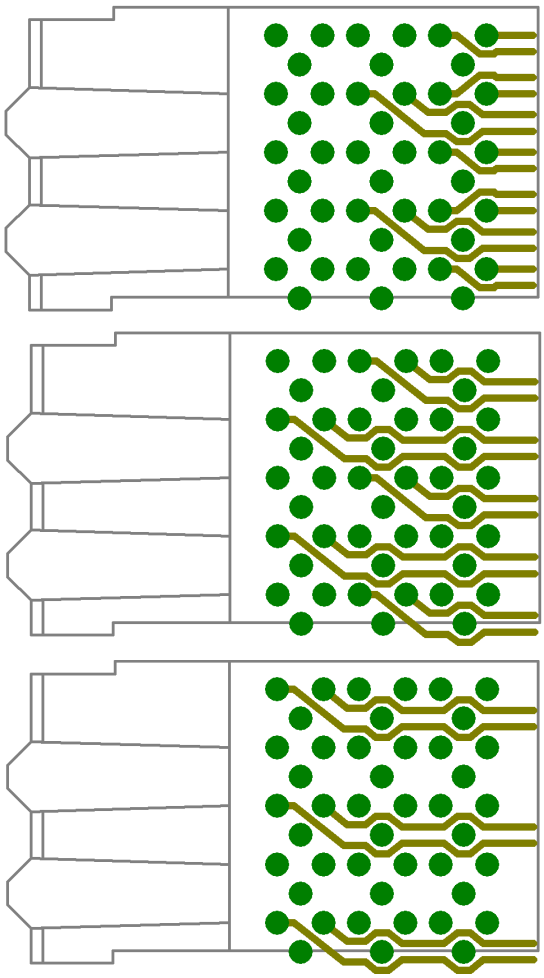


Figure 13: Daughtercard Differential Breakout Pattern (3 Layers)

2. Z-PACK HS3 10 Row Breakout

On a daughter card, the 10 row version of the Z-PACK HS3 requires **5 signal layers** (also with some free remaining channels), while the motherboard (or backplane) requires a minimum of **2 signal layers** to route out. Examples of typical breakout patterns for the Z-PACK HS3 10 row connector pinfields are shown in Figure 14 – Figure 16.

Backplane

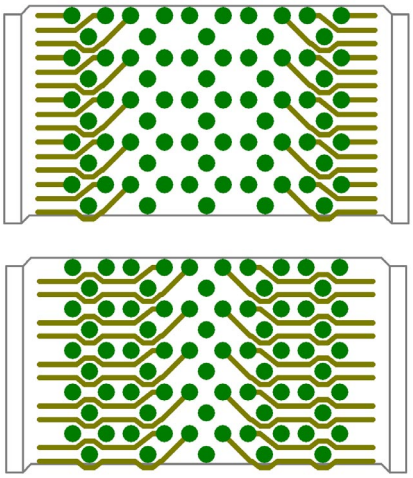


Figure 14 : Backplane Single-Ended Breakout Pattern (2 Layers)

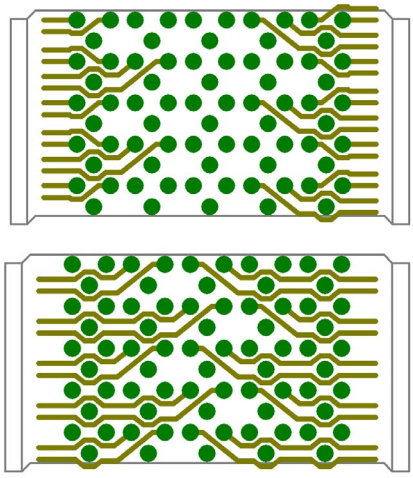


Figure 15: Backplane Differential Breakout Pattern (2 Layers)

Daughtercard

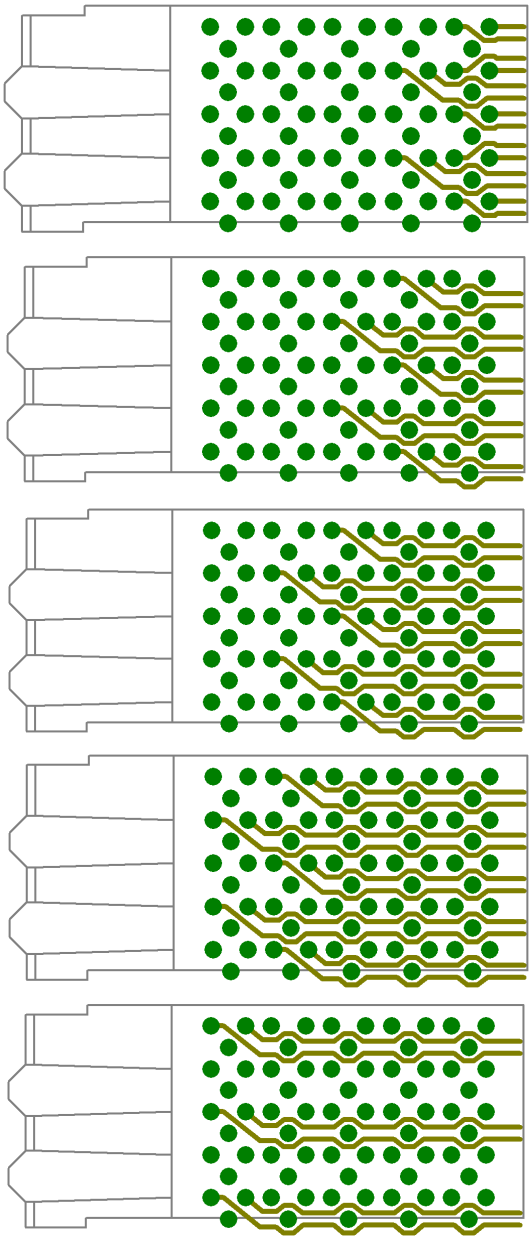


Figure 16: Daughtercard Differential Breakout Pattern (5 Layers)

V. Electrical Performance

Electrical performance reports which contain validated crosstalk data for the connector, are available for the AMP Z-PACK HS3 connector. Additional test and simulation data showing throughput capabilities of the Z-PACK HS3 connector is also available. Both types of reports are available at www.amp.com/simulation. The electrical performance impact of routing traces through the Z-PACK HS3 footprint is covered in the sections below.

A. Antipad Adjacency

In some cases where wide traces are routed through the connector footprint the reference plane clearance (antipad) will partially overlap areas of the routed trace. However, the impact on trace impedance and noise generation is minor due to the short electrical length of the overlap. Traces routed in the Z-PACK HS3 footprint maintain full reference plane coverage except where routing over the antipad is required. Figure 17 shows the effects of routing wide traces over large antipads in the Z-PACK HS3 footprint. The frequency response of a standard stripline trace not routed through pinfields is compared with an identical trace routed through 12 footprints. The difference between the two response curves is negligible.

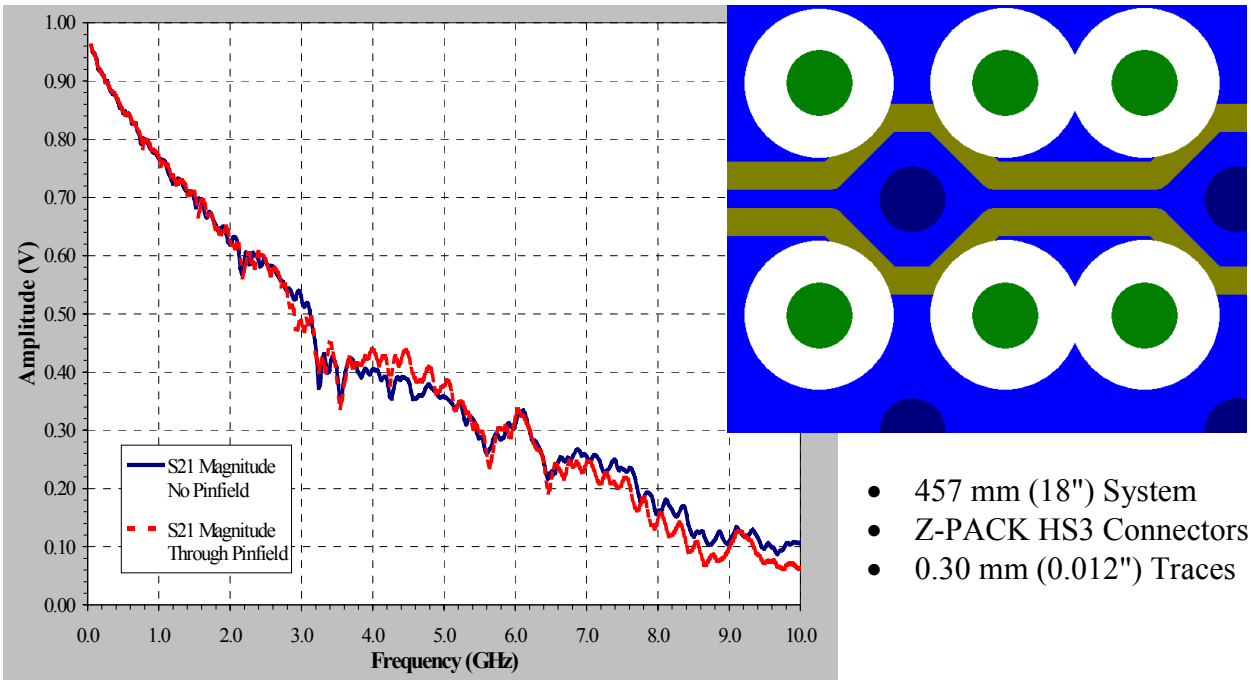


Figure 17: Measured Performance of Routing Over Antipads

This routing effect as viewed in the time domain manifests as an impedance discontinuity. Figure 18 and Figure 19 show that the impedance variation due to trace jogging and routing over antipads is only 3 Ω as measured by an unfiltered TDR. The

figures show that the trace impedance variation due to manufacturing is comparable to the antipad discontinuity. Figure 18 shows the 0.30 mm (0.012") wide trace routed for a distance of 305 mm (12") across a two-daughtercard system. Figure 19 represents the same trace routed for 305 mm (12") through 12 Z-PACK HS3 pinfields. Both figures are centered around a 50 Ω impedance offset.

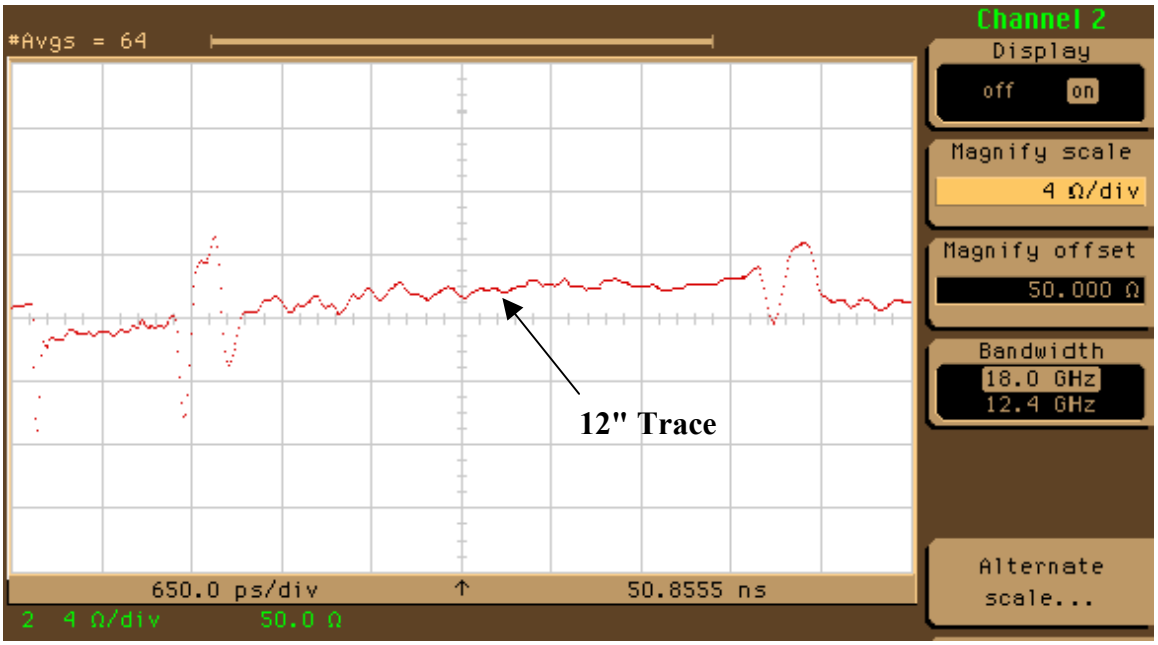


Figure 18: Routing Impedance (Trace Only)

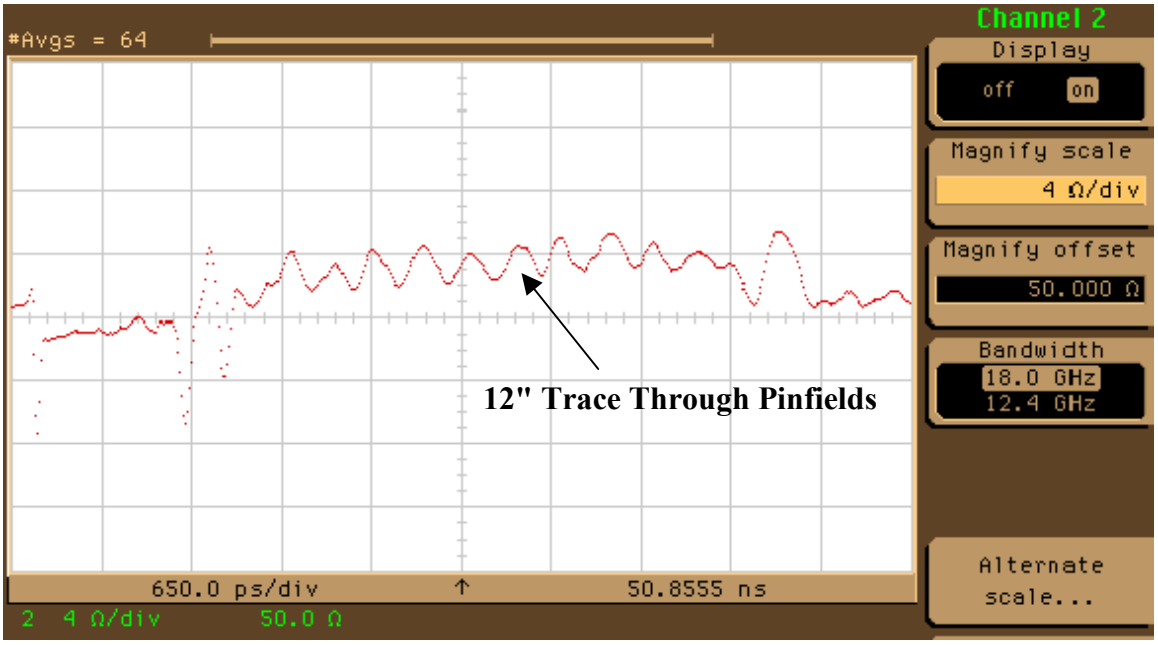


Figure 19: Routing Impedance (Through Pinfields)

As a result, reducing the overlap of the trace and antipad minimizes discontinuities on the signal. When connecting traces to signal pins, the entire trace must route over the antipad for a short distance. To minimize the antipad discontinuity entire traces should be routed over antipads for as short a distance as possible. Additionally, entire traces should not cross other antipads or ground clearances, but maintain a continuous adjacent-layer ground path in the Z-PACK HS3 footprint.

B. Differential Pair Coupling

For edge-coupled differential signals, trace jogging is necessary around the ground pins of the connector footprint. These differential signals which must separate, will still maintain a consistent differential impedance in that region of the connector. Figure 20 and Figure 22 show TDR plots of the differential impedance of both loosely spaced (<5% trace-to-trace coupling) and closely spaced (>20% trace-to-trace coupling) differential pairs routed across 305 mm (12") of backplane. Figure 21 and Figure 23 show the same two trace geometries routed through 12 Z-PACK HS3 pinfields. The differential impedance scale of all four figures is 80mρ / division (approximately 8 Ω / division). The four figures show that the impedance varies only ~ 4 Ω from the nominal 100 Ω (well within standard board manufacturing constraints of 10%) as measured by an unfiltered TDR. By designing the differential pairs that are primarily coupled to ground, Z-PACK HS3 footprint differential routing is able to closely maintain a 100 Ω differential trace impedance.

C. Skew & Propagation Delay

As a right-angle connector, each row of the Z-PACK HS3 has a different electrical path length. Typical values are provided below in the single line model data of AMP connectors. Figure 24 and Figure 25 are current single line model data sheets for the AMP Z-PACK HS3 connector. All electrical and mechanical information should be verified that it is current and applicable (www.amp.com/simulation). Although it is possible to assign differential signals in-row to reduce skew, this is not recommended because the noise-shielding effectiveness of the in-column ground blades is greatly reduced.

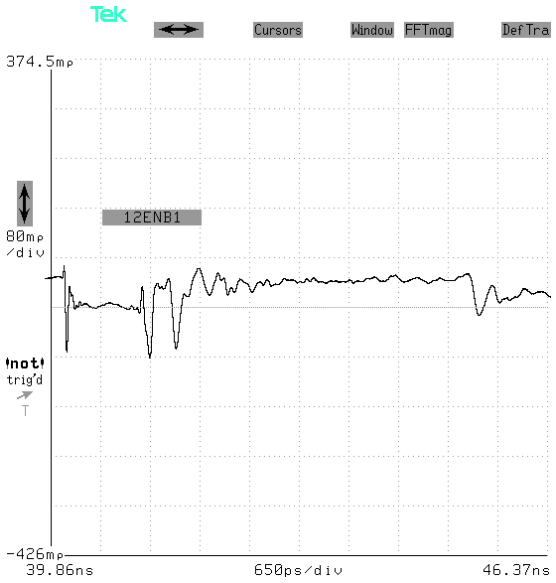


Figure 20: Loosely Coupled Signal Pair

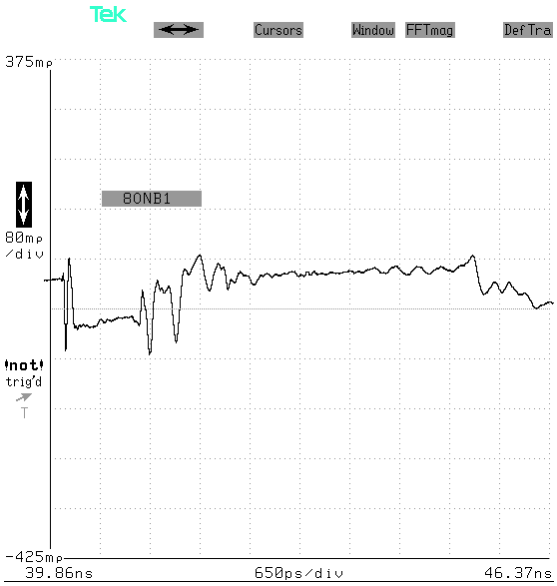


Figure 22: Tightly Coupled Signal Pair

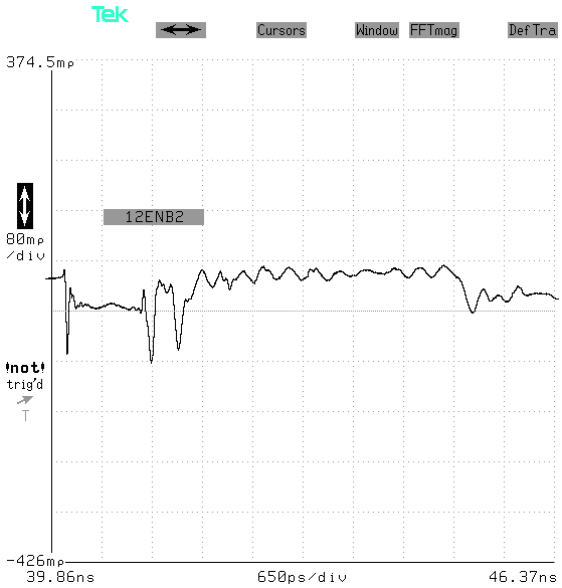


Figure 21: Loosely Coupled Signal Pair Routed Through Pinfields

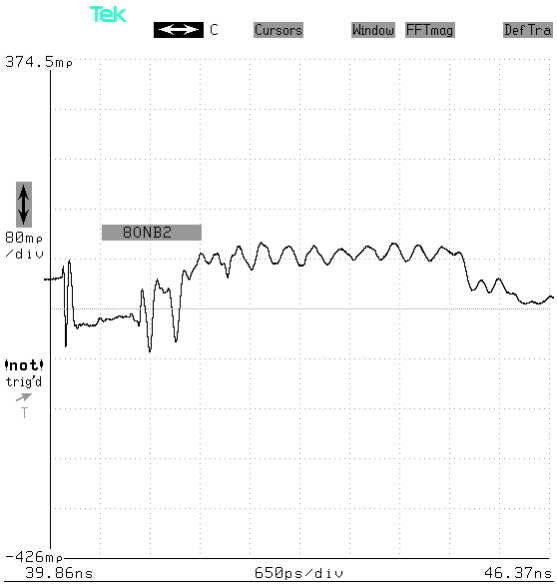


Figure 23: Tightly Coupled Signal Pair Routed Through Pinfields

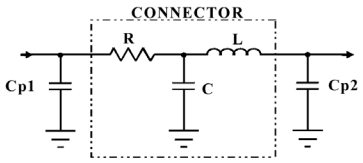
AMP SINGLE LINE MODEL DATASHEET

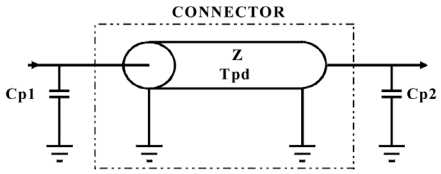
ZPACK HS3, 2.5mm Pitch, 6 Row, Vertical Plug to Right Angle Receptacle (Dual Beam Contact)

VALIDATED

All Signal pattern

Model Boundaries: Board Surface to Board Surface





Connector Lumped Constant Model

Row	R (mΩ)	L (nH)	C (pF)
A	12	4.73	1.40
B	14	5.21	1.81
C	16	5.98	2.11
D	18	6.75	2.46
E	20	7.53	2.77
F	22	8.72	3.03

Connector Distributed Model

Z (Ω)	Tpd (ps)
58	81
54	97
53	112
52	129
52	144
54	163

Note: (1) The following RLC model is appropriate for edge speeds slower than ten times the highest propagation delay (Tr>=10 * Tpd(highest)). To accommodate faster edge speeds, the lumped model must be divided into two or more RLC sections. For best results, a section's propagation delay should be $1/10^{th}$ of the edge speed.

(2) The single line inductance and capacitance values are extracted from a specified pattern. The placement and number of ground returns affect the inductance and capacitance of the single line model.

(3) The parameters for the Single Line Model are for the connector only without any mounting effects such as plated through holes or pads capacitance (Cp1 and Cp2). The impedance and propagation delay for the connector are calculated as follows:

$$Z_{Connector} = \sqrt{\frac{L}{C}}(\Omega) \text{ and } Tpd_{Connector} = \sqrt{L*C}(sec)$$

For an interconnection path model, the mounting effects must be added because the additional capacitance of the pad to ground or plated through hole (Cp1 and Cp2) decrease impedance and increase propagation delay of the interconnection path. The impedance and propagation delay for an interconnection path are calculated as follows:

$$Z_{Interconnect} = \sqrt{\frac{L}{C+(Cp1+Cp2)}}(\Omega) \text{ and } Tpd_{Interconnect} = \sqrt{L*(C+Cp1+Cp2)}(sec)$$

FOR ADDITIONAL ELECTRICAL MODELING/SIMULATION SUPPORT,
E-MAIL US AT modeling@tycoelectronics.com, OR VISIT OUR WEBSITE AT www.amp.com/simulation

Datasheet Filename: SLM-1999-3681-051A.doc
Created on 10/13/00

Reviewed By: [CTK]
Modeled by: [DWG]

Figure 24: AMP Z-PACK HS3 6 Row Single Line Data

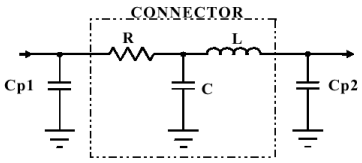
AMP SINGLE LINE MODEL DATASHEET

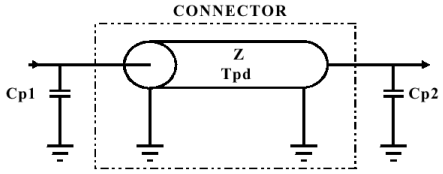
ZPACK HS3, 2.5mm Pitch, 10 Row, Vertical Plug to Right Angle Receptacle (Dual Beam Contact)

VALIDATED

All Signal pattern

Model Boundaries: Board Surface to Board Surface





Connector Lumped Constant Model

Row	R (mΩ)	L (nH)	C (pF)
A	12	4.61	1.41
B	14	5.06	1.82
C	16	5.84	2.13
D	18	6.63	2.45
E	20	7.41	2.76
F	22	8.20	3.11
G	24	8.95	3.44
H	26	9.73	3.78
J	28	10.52	4.12
K	30	12.31	4.19

Connector Distributed Model

Z (Ω)	Tpd (ps)
57	81
53	96
52	112
52	127
52	143
51	160
51	175
51	192
51	208
54	227

Note: (1) The following RLC model is appropriate for edge speeds slower than ten times the highest propagation delay (Tr>=10 * Tpd(highest)). To accommodate faster edge speeds, the lumped model must be divided into two or more RLC sections. For best results, a section's propagation delay should be $1/10^{th}$ of the edge speed.

(2) The single line inductance and capacitance values are extracted from a specified pattern. The placement and number of ground returns affect the inductance and capacitance of the single line model.

(3) The parameters for the Single Line Model are for the connector only without any mounting effects such as plated through holes or pads capacitance (Cp1 and Cp2). The impedance and propagation delay for the connector are calculated as follows:

$$Z_{Connector} = \sqrt{\frac{L}{C}}(\Omega) \text{ and } Tpd_{Connector} = \sqrt{L*C}(sec)$$

For an interconnection path model, the mounting effects must be added because the additional capacitance of the pad to ground or plated through hole (Cp1 and Cp2) decrease impedance and increase propagation delay of the interconnection path. The impedance and propagation delay for an interconnection path are calculated as follows:

$$Z_{Interconnect} = \sqrt{\frac{L}{C+(Cp1+Cp2)}}(\Omega) \text{ and } Tpd_{Interconnect} = \sqrt{L*(C+Cp1+Cp2)}(sec)$$

FOR ADDITIONAL ELECTRICAL MODELING/SIMULATION SUPPORT,
E-MAIL US AT modeling@tycoelectronics.com, OR VISIT OUR WEBSITE AT www.amp.com/simulation

Datasheet Filename: SLM-1999-3681-066.doc
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Reviewed By: [CTK]
Modeled by: [DWG]

Figure 25: AMP Z-PACK HS3 10 Row Single Line Data

VI. Summary

Table 2 is provided to summarize the recommendations presented in this document.

Item	Value
Connector Dimensions:	
Z-PACK HS3 Signal Pin Column Pitch	2.5 mm (0.098")
Z-PACK HS3 Signal Pin Row Pitch	1.5 mm & 2.0 mm (0.059") & (0.079")
Number of Connector Rows	6 and 10
Number of Connector Columns	5 and 10
Footprint Dimensions:	
Suggested Pad Size	≥1.02 mm (0.040")
Suggested Antipad Size Range	1.27 mm – 1.60 mm (0.050") – (0.063")
Maximum Trace Width (Plug & Receptacle)	0.30 mm (0.012")
Nominal Finished Hole Size	0.60 mm (0.024")
Nominal Drill Hole Size	0.70 mm (0.0276")
Copper Thickness in Hole	0.0375 mm ± 0.0125 mm (0.0015" ± 0.0005")
Layer Requirements:	
Layers Required to Fully Route out of a 6 Row Z-PACK HS3 on a Backplane	1
Layers Required to Fully Route out of a 10 Row Z-PACK HS3 on a Backplane	2
Layers Required to Fully Route out of a 6 Row Z-PACK HS3 on a Daughtercard	3
Layers Required to Fully Route out of a 10 Row Z-PACK HS3 on a Daughtercard	5
Pad Size Required to Quad Track Route 0.005"/ 0.005" Traces/Spaces	0.94 mm (0.037")
Electrical Propagation Data:	
6 Row Z-PACK HS3 Typical Electrical Propagation of "A" Row Pin	81 ps
6 Row Z-PACK HS3 Typical Electrical Propagation of "B" Row Pin	97 ps
6 Row Z-PACK HS3 Typical Electrical Propagation of "C" Row Pin	112 ps
6 Row Z-PACK HS3 Typical Electrical Propagation of "D" Row Pin	129 ps
6 Row Z-PACK HS3 Typical Electrical Propagation of "E" Row Pin	144 ps
6 Row Z-PACK HS3 Typical Electrical Propagation of "F" Row Pin	163 ps
10 Row Z-PACK HS3 Typical Electrical Propagation of "A" Row Pin	81 ps
10 Row Z-PACK HS3 Typical Electrical Propagation of "B" Row Pin	96 ps
10 Row Z-PACK HS3 Typical Electrical Propagation of "C" Row Pin	112 ps
10 Row Z-PACK HS3 Typical Electrical Propagation of "D" Row Pin	127 ps
10 Row Z-PACK HS3 Typical Electrical Propagation of "E" Row Pin	143 ps
10 Row Z-PACK HS3 Typical Electrical Propagation of "F" Row Pin	160 ps
10 Row Z-PACK HS3 Typical Electrical Propagation of "G" Row Pin	175 ps
10 Row Z-PACK HS3 Typical Electrical Propagation of "H" Row Pin	192 ps
10 Row Z-PACK HS3 Typical Electrical Propagation of "J" Row Pin	208 ps
10 Row Z-PACK HS3 Typical Electrical Propagation of "K" Row Pin	227 ps

Table 2: Data Summary

Table 3 through Table 6 provide representative padstack recommendations based upon typical system goals. The padstack recommendations are only suggested values, that may or may not be applicable to any given system and should be evaluated before use.

Item	Value
Suggested Pad Size	1.02 mm (0.040")
Suggested Antipad Size	1.60 mm (0.063")

Table 3: High Speed Padstack Recommendations

Item	Value
Suggested Pad Size	1.02 mm (0.040")
Suggested Antipad Size	1.27 mm (0.050")

Table 4: Low Noise Padstack Recommendations

Item	Value
Suggested Pad Size	1.07 mm (0.042")
Suggested Antipad Size	1.42 mm (0.056")

Table 5: Nominal Padstack Recommendations

Item	Value
Suggested Pad Size	1.12 mm (0.044")
Suggested Antipad Size	1.60 mm (0.063")

Table 6: High Volume Production (Conservative) Padstack Recommendations

VII. Related Documents

- A representative Cadence Allegro and Mentor Falcon part model is available based upon the design parameters specified in this reference document.
- Electrical models of the Z-PACK HS3 connector are available at www.amp.com/simulation.
- Reference designs and conference papers are available at www.amp.com/simulation.
- Mechanical detailed drawings of the AMP Z-PACK HS3 connector are available at www.amp.com.

VIII. Contact Information

A. Tyco Electronics

Tyco Electronics Corporation is the world's leader in electrical, electronic and fiber-optic connectors and interconnection systems. Its facilities are located in over 50 countries serving customers in the automotive, computer, communications, consumer electronics, industrial and power industries. Tyco Electronics, headquartered in Harrisburg, Pennsylvania, USA, is the largest passive electronics components supplier in the world, providing advanced technology products from its AMP, Elcon, Elo Touchsystems, HTS, M/A-COM, Madison Cable, OEG, Potter & Brumfield, Raychem, Schrack and Simel brands.

For more information about TYCO Products, call us today or visit us on the web.

Product Information Center	800-522-6752 717-986-7777
Internet	http://www.tycoelectronics.com

B. Communications Circuits & Design

Communications Circuits & Design (CC&D) is part of the Global Communications Business Unit of Tyco Electronics, which focuses on the rapidly growing telecom and networking markets. CC&D offers the industry interconnection expertise from concept to production, and helps customers to validate their designs at the concept stage. CC&D is providing a leadership role for the industry in the area of signal integrity by working with Tyco Electronics customers, industry standard working groups, and semiconductor vendors.

Offering interconnection expertise from concept to production, CC&D can help validate your design and package it for manufacturing. At the front end, our end-to-end computer simulation and analysis of your system will evaluate the most critical parameters of your design. Our advanced analysis and modeling techniques can help determine the optimal device drivers, board design and stackup, and board layout for your design. By identifying problems such as reflections, ground bounce, crosstalk, jitter, propagation delay, and timing, CC&D can help you reduce costs and verify the performance of your design.

CC&D has been instrumental in developing and verifying many of the world's most popular bus standards. Here is a brief sampling.

CompactPCI: Our recommendations helped make CompactPCI the rock-solid, industrial-strength bus that combines high performance with flexibility.

CompactPCI Hot Swap: We provided the critical simulations that allowed mission-critical hot swapping to be a reality in CompactPCI.

CT: CC&D performed the simulations for the H.110 computer telephony extensions to CompactPCI.

PXI: Our analysis of PXI resulted in several improvements for increased signal integrity.

CPCI/CT/ATM Backplane: This is a CC&D-designed system that combines CompactPCI, CT, and *Cellbus* into a high-performance system that meets the growing needs of communications convergence.

To find out more about our design services, contact us today.

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Electrical models	modeling@amp.com