EE273 Digital Systems Engineering
Final Exam

December 10, 1998
(version 1.0)

(Total time = 120 minutes, Total Points = 100)

Name: (please print)_____

In recognition of and in the spirit of the Stanford University Honor Code, I certify that I will neither give nor receive unpermitted aid on this exam.

Signature:_____

This examination is open notes open book. You may not, however, collaborate in any manner on this exam. You have two hours to complete the exam. Please do all of your work on the exam itself. Attach any additional pages as necessary.

Before starting, please check to make sure that you have all 9 pages.

1		**30**
2		**15**
3		**15**
4		**12**
5		**12**
6		**16**
Total		**100**

Problem 1: Short Answer (30 Points: 6 questions, 5 points each)

A. Suppose you have a brute-force asynchronous arbiter with a flip-flop time constant, τ_s, of 100ps and a waiting time, t_w, of 10ns that has a synchronization failure once per second. What will the failure rate be if you double the waiting time to 20ns?

B. A signal, A, is synchronized to a 50MHz clock. You wish to bring A into a clock domain synchronized to a 33MHz clock. What type of synchronizer is called for? What is the minimum synchronization delay?

C. What timing convention is more tolerant of clock skew, (a) edge-triggered timing, or (b) two-phase level-sensitive timing.

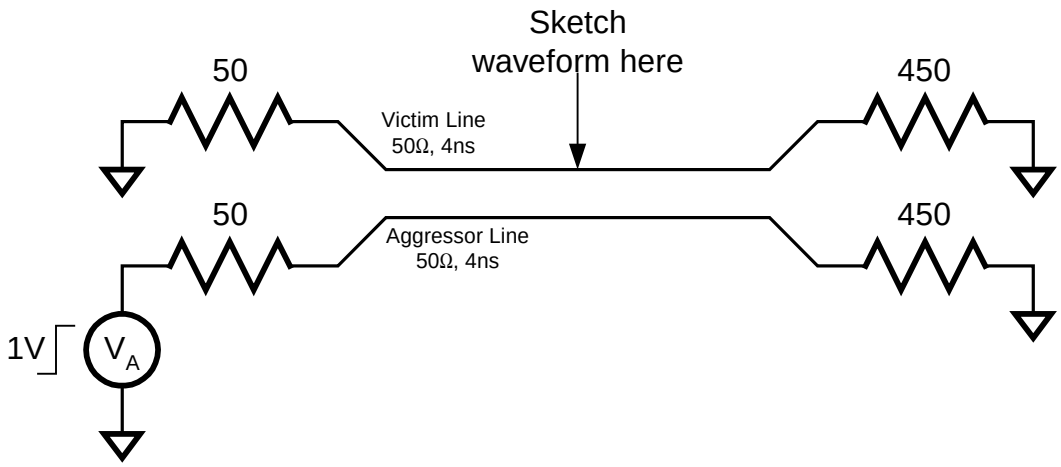
D. With a large, local bypass capacitor on-chip near the point of use, an on-chip power distribution network must be sized for the (a) peak, or (b) average current drawn during a maximum power cycle?

E. Consider a mesochronous synchronizer and a plesiochronous synchronizer with identical parameters. The plesiochronous synchronizer has a failure rate of 1×10^{-40} s^{-1}. What is the failure rate of the mesochronous synchronizer? Explain (10 words or less).

F. A signaling system has a rise/fall time of 50ps, an aperture time of 50ps, peak-to-peak jitter of 150ps (combined receiver and transmitter jitter), and operates over a line with 800ps of delay. What is the fastest rate at which this signaling system can operate?

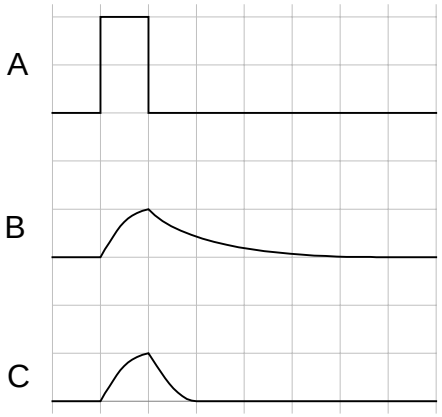
Problem 2: Transmission Lines [15 Points]

A pair of 50Ω transmission lines are terminated as shown in the drawing below. The lines are coupled over their entire 4ns length with a forward crosstalk coefficient, k_{fx}, of 0 and a reverse crosstalk coefficient, k_{rx}, of 5%. The *aggressor* line is driven with a 1V step with a 100ps rise time as shown. Sketch and dimension the voltage waveform at the midpoint of the victim line.

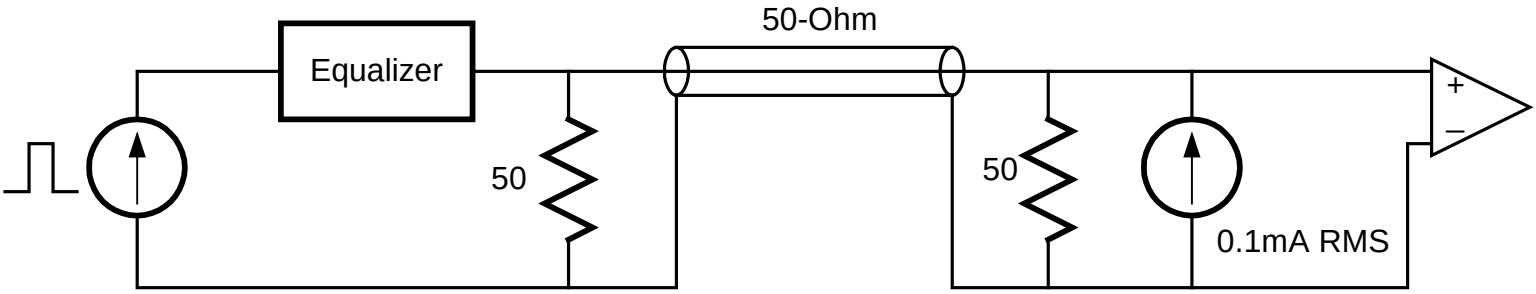


Problem 3: Signaling and Noise Analysis [15 points total]

Consider a signaling system where the transmission medium has the pulse response show on line B below. The waveform shows the response at the far end of the line to a one-bit wide pulse of unit magnitude (line A). The pulse response (line B) has magnitude of 0.50, 0.20, 0.1, and 0.06 at the end of the first four bit times after the start of the pulse. After the fourth bit time, the pulse response is essentially zero. By inserting a linear equalizing filter into our signaling system (at either end of the line) we generate the equalized pulse response shown on line C. This equalized response has a magnitude of 0.50 at the end of the first bit time and zero at the end of all other bit times.

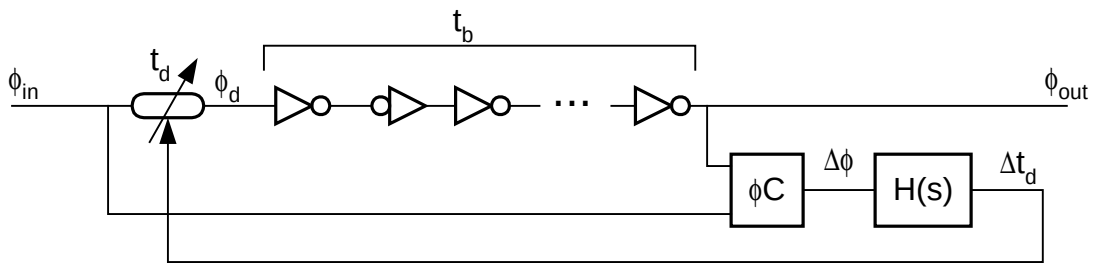


Part A: [8 points] The equalizer described above is being used in a signaling system as shown below. The receiver has 50mV sensitivity and 0mV of offset. There is 0.1mA RMS of Gaussian noise added to the signal on the 50-Ohm medium. Also, the transmission line is terminated into 50-Ohms at both ends. What is the lowest peak signal current at the transmitter (on the output of the equalizer) that gives a BER of 10^{-9} or lower?



Part B [7 points]: Design a two-tap FIR equalizer that best approximates the ideal equalizer described above.

Problem 4: Timing: Residual Error [12 points total]

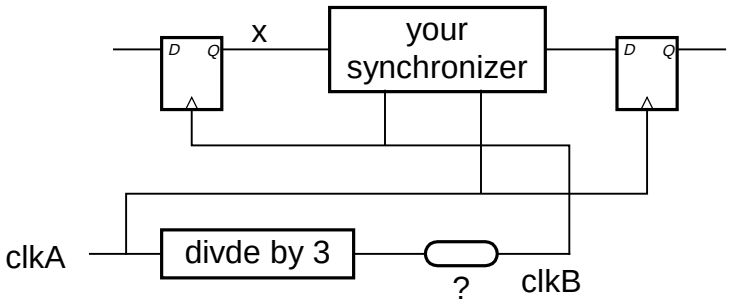


Consider the simple closed-loop, zero-delay buffer design shown above. You are designing this buffer for use with a 500MHz clock (ϕ_{in}). It must operate across process corners. Your voltage-controlled delay line varies its delay linearly from 200ps to 1ns as the control voltage is varied from a 3.0V maximum down to a 1.4V minimum (for a gain of 0.5ns/V). Your phase comparator outputs 2.2V when its two inputs are exactly in phase and has a gain of 2V/ns in its linear region. The loop filter is a unity-gain low-pass filter. The buffer delay, t_b, is 700ps at the slow corner and 300ps at the fast corner. For the purpose of this problem, assume that the performance of all other loop components is constant across process corners.

Part A: [6 points] What is the residual phase error (in ns) at the slow corner? (Hint: do **not** just blindly apply equation (9-35) from the book. Think.)

Part B: [6 points] What is the residual phase error (in ns) at the fast corner?

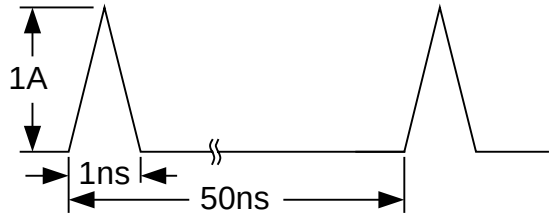
Problem 5: Synchronization [12 points total]



Part A [5 points]: Consider the circuit shown above. A 300MHz clock, clkA, is divided by three and delayed by an arbitrary amount to generate a 100MHz clock, clkB. What type of synchronizer is needed to move a signal, x, that is synchronized with clkB into the domain of clkA?

Part B [7 points]: Sketch an implementation of a synchronizer for the situation of part A.

Problem 6: Power Distribution [16 points total]



Part A: [6 points] Suppose you have a subsystem on your chip that draws current with the profile shown above. The current is drawn in a triangle wave with a duration of 1ns. The peak value is 1A. The time between pulses is 50ns (the drawing is not to scale on the time axis), so the average value is 10mA. (If you need parameter k_i for this waveform, you may assume it is 1.0). Your subsystem is connected to the power supply via a pair of networks (one for GND and one for V_{DD}) that are modeled as two 1-Ohm resistors. What is the smallest value local bypass capacitor that is needed at your subsystem to keep the voltage ripple on a 2.5V supply to within 10%?

Part B: [5 points] Suppose you have a chip that draws the current waveform from part A above and may start or stop operation in a single clock cycle. The chip is connected to the power supply via a network that is modeled as a single 10nH inductor (combining the effects of the GND and V_{DD} inductances). You may ignore the resistive part of the network for this part of the problem (and for part C). What is the smallest bypass capacitor that will hold the voltage ripple at the input of the chip to 10% of the 2.5V supply?

Part C: [5 points] Suppose you insert a linear series regulator in the supply network from Part B as shown below. If the distribution voltage is 3.3V and the supply voltage is 2.5V, what is the minimum-sized bypass capacitor that will hold the 2.5V supply to within 10% (assume that the regulator is ideal)? What is the increase in total power dissipated? How high a voltage must the bypass capacitor be able to withstand?