EE273 Digital Systems Engineering
Final Exam

March 16, 2000
(version 0.4δ)

(Total time = 120 minutes, Total Points = 100)

Name: (please print)_____

In recognition of and in the spirit of the Stanford University Honor Code, I certify that I will neither give nor receive unpermitted aid on this exam.

Signature:_____

This examination is open notes open book. You may not, however, collaborate in any manner on this exam. You have two hours to complete the exam. Please do all of your work on the exam itself. Attach any additional pages as necessary.

Before starting, please check to make sure that you have all 9 pages.

1		**20**
2		**15**
3		**16**
4		**24**
5		**25**
Total		**100**

Problem 1: Short Answer (20 Points: 10 questions, 2 points each)

A. Suppose you have a signaling system with Gaussian noise of 10mV RMS and a BER of 10^{-20}. If you double the Gaussian noise to 20mV, what will the new BER be?

B. In a signaling system where the line is terminated at both ends into a matched impedance, what is the percentage of ISI caused by a 10% terminator mismatch at both ends?

C. A brute force synchronizer uses a flip-flop with an aperture time of 100ps and a regeneration time constant of 100ps driven by a 1GHz clock. The synchronizer currently uses a waiting time, t_w, that gives a failure rate of 10^{-10}. If you double this waiting time, what will the new failure rate be?

D. A system employs synchronous timing and stacks three bits on the transmission line between two modules. What should the relationship be between the delay of the transmission line and the bit time to center the clock on the eye? (For the purposes of this problem, assume zero t_{dCQ} and zero rise/fall time.)

E. To avoid dropping or duplicating symbols, when is a plesiochronous FIFO synchronizer allowed to adjust its read pointer?

F. A two-register plesiochronous synchronizer moves a signal between two 100MHz +/- 100ppm clock domains. What is the minimum frequency at which the synchronizer register selection must be updated?

G. A pipelined timing system operates at the maximum possible rate of 1Gb/s over a 10ns line. If the length of the line is doubled while all other parameters (rise-time, aperture, skew, and jitter) remain constant, what is the new maximum signaling rate? (Assume that attenuation of the longer line is not a factor.)

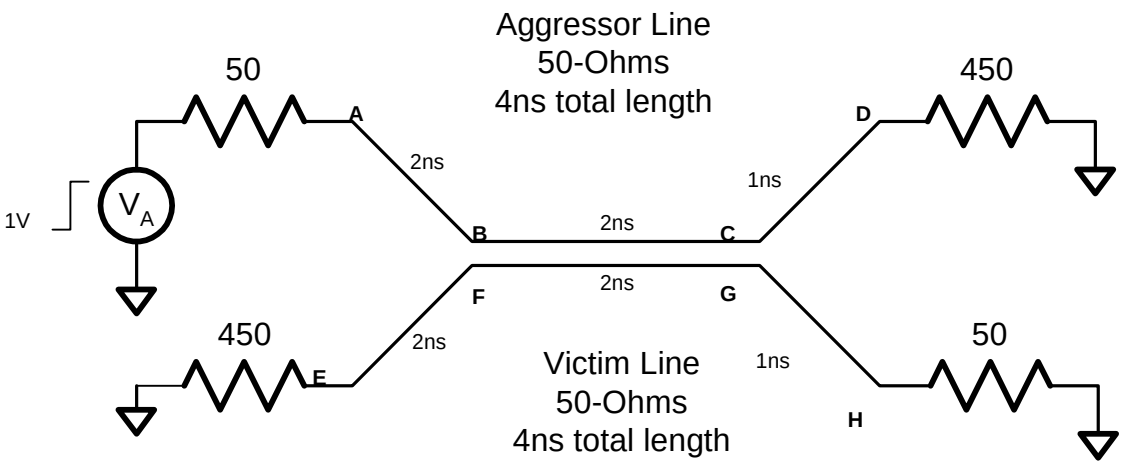
H. If the peak-to-peak timing uncertainty in the system of problem (G) is doubled from 300ps to 600ps what happens to the maximum signaling rate?

I. On chip clock distribution is easier than off chip clock distribution because the on-chip wires are of much higher quality (true or false)?

J. A brute force synchronizer has a failure probability of 10^{-30}. If the aperture time of a flip-flop used as the first stage of a brute force synchronizer is doubled while all other parameters (including the regeneration time constant of the flip-flop) are held constant, what will the new failure probability be?

Problem 2: Transmission Lines [15 Points]

A pair of 50Ω transmission lines are terminated as shown in the drawing below. The lines are coupled over 2ns of their 4ns length with a forward crosstalk coefficient, k_{fx}, of 0 and a reverse crosstalk coefficient, k_{rx}, of 10%. The *aggressor* line is driven with a 1V step with a 100ps rise time as shown. Sketch and dimension the voltage waveform at point H, the far end of the victim line. (You need not consider any waves that have a magnitude less than 10mV).



Problem 3: Signaling [16 points total]

Consider the current mode signaling system shown below. The system uses 1mA to signal a "1" and –1mA to signal a "0". The data rate is 1Gb/s and transitions have a 500ps rise/fall time. The line is terminated at both ends with resistors that are matched to the 50-Ohm line with a 10% tolerance. The line is an ideal 50-Ohm line with a single discontinuity, a 1pF capacitor midway along its 4ns length. The line is coupled to an adjacent line carrying a signal in the same direction with a forward crosstalk coefficient, k_{fx}, of 0 and a reverse crosstalk coefficient, k_{rx}, of 10%. For purposes of this question, assume that the receiver and transmitter are perfect.

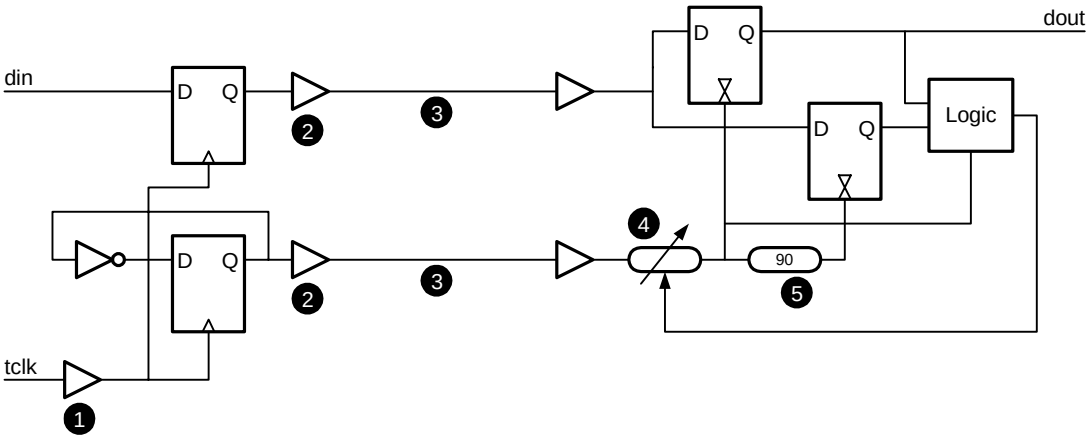
A. (8 pts) For each of the noise sources listed below, give the magnitude of the noise **at the receiver** due to that source:

Noise Source	**Magnitude of Noise at the Receiver**
Far-end crosstalk	
Near-end crosstalk	
ISI due to termination mismatch (both ends)	
Impedance discontinuity	

B. (8 pts) Now suppose you remove the source termination. List the sources for which the receiver noise changes and the new value of the noise at the receiver due to each of these sources:

Noise Source	**Magnitude of Noise at the Receiver**

Problem 4: Timing [24 points total]



The figure above illustrates a 1Gb/s closed loop timing system with five sources of delay, skew, and jitter identified by white numbers in black circles. The sources are:

No	Description	Delay	Skew	Jitter (p-p)
1	Transmit clock buffer tree	2000ps	N/A	200ps
2	Transmit flip flops and drivers	500ps	25ps	50ps
3	Transmission line	2000ps	200ps	0ps
4	Variable delay	100-600ps	N/A	10%
5	Fixed 90-degree delay	500ps	50ps	50ps

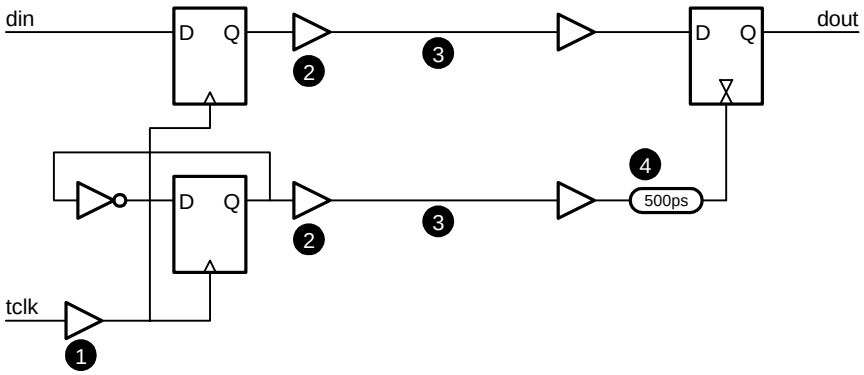
Note that skew for a single element (like 5) refers to variation from nominal delay while skew for a pair of elements (2 and 3) refers to the difference between the two elements. Also note that skew is a magnitude (e.g., 50ps means +/- 50ps from the nominal value) and jitter is given as peak-to-peak.

The system operates by using a 1GHz transmit clock, tclk, to clock both a data flip-flop (top) and a toggle flip-flop (bottom) that generates a 500MHz reference clock. Jitter in the transmit flip-flops is completely correlated. That is, if the delay of the upper flip-flop is increased by 25ps, the delay of the lower flip-flop is increased by the same amount. The data and reference clock are transmitted over parallel transmission lines that are matched to within 200ps. At the receiver the reference clock is delayed by a variable delay line to center it on the data eye and used to clock a double-edge-triggered flip-flop to recover the data. The clock is delayed by a further 90-degrees (to sample the edge) and used to clock another double-edge triggered flip-flop. A logic block (which may include additional flip-flops) uses the two data samples to control the variable delay line.

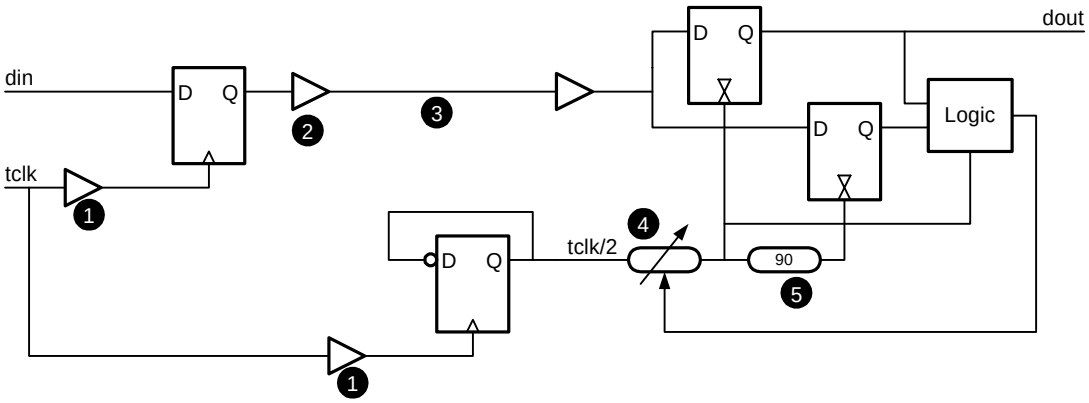
A. (8 points) Which of the skew and jitter sources listed above contribute to the overall uncertainty of the timing system? That is, which are not compensated by the design of the system? Circle the contributing elements in the table below:

No	Description	Delay	Skew	Jitter
1	Transmit clock buffer tree	2000ps	N/A	200ps
2	Transmit flip flops and drivers	500ps	25ps	50ps
3	Transmission line	2000ps	200ps	0ps
4	Variable delay	100-600ps	N/A	10%
5	Fixed 90-degree delay	500ps	50ps	50ps

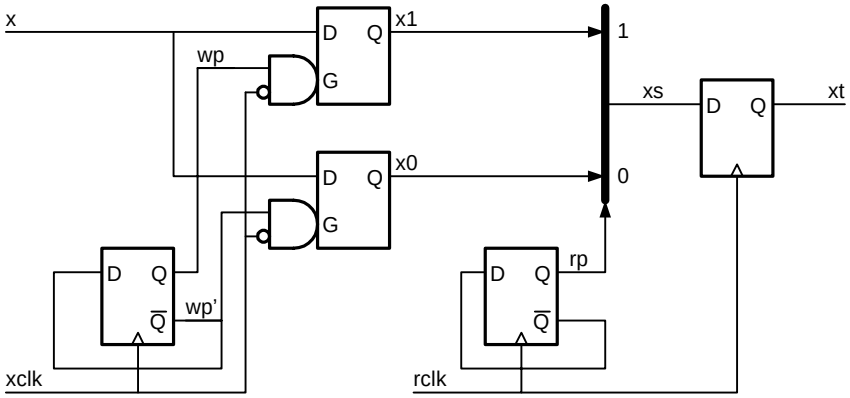
B. (8 points) Consider the revised system below where the variable delay line is replaced by a fixed 500ps delay. How does this change how the five elements above contribute to timing uncertainty. List the elements that change:



C. (8 points) Now consider returning to the original system (of part A) but replacing the reference clock by a mesochronous tclk/2 signal at the receiver. Compared to the system of part A, how does this change how the five elements above contribute to timing uncertainty. List the elements that change:

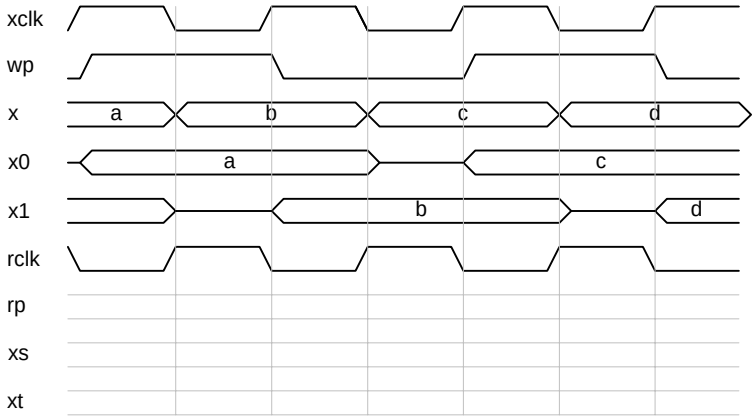


Problem 5: Synchronization [25 points total]



The picture above illustrates a two-element FIFO synchronizer constructed with latches rather than flip-flops. Signal x, synchronized to xclk is sampled alternately into two latches, generating x0 and x1 under control of a write pointer, wp, generated by a toggle flip-flop clocked by xclk. Signals x0 and x1 are input to a multiplexer controlled by the read pointer, rp (when rp=1 the upper input is selected). The read pointer is generated by a toggle flip-flop clocked by the receiver clock, rclk. Finally, the output of the multiplexer is clocked into an output flip-flop by rclk. (You may assume that t_{cCQ} of the flip-flop is significantly greater than t_h and that there is zero clock skew within one clock domain (but there is arbitrary skew between tclk and rclk). Also assume that the multiplexer delay is zero.)

A. (8 points) The timing diagram below gives the timing of xclk, x, wp, x1, x0, and rclk for the case where rclk is 180 degrees out of phase with xclk. Complete the diagram by sketching the waveforms for rp, xs, and xt. (The shaded lines are provided to guide your sketch).



B. (8 points) What is the timing relationship that must hold between the write pointer, wp, and the read pointer, rp for the system to operate properly? Express your answer as one or more inequalities on the phases of the two signals.

C. (9 points) Sketch a circuit that could be used to correctly generate rp in the case where rclk and xclk are plesiochronous. Assume that you have a signal 'bothnull' that indicates when there are null symbols in both flip-flops and that this condition is guaranteed to occur often enough.