

# EE273 Digital Systems Engineering Midterm Exam

February 9<sup>th</sup>, 2000

**(Total time = 120 minutes, Total Points = 100)**

Name: (please print) \_\_\_\_\_

In recognition of and in the spirit of the Stanford University Honor Code, I certify that I will neither give nor receive unpermitted aid on this exam.

Signature: \_\_\_\_\_

**This examination is open notes open book. You may not, however collaborate in any manner on this exam. You have two hours to complete the exam. Please do all of your work on the exam itself. Attach any additional pages as necessary.**

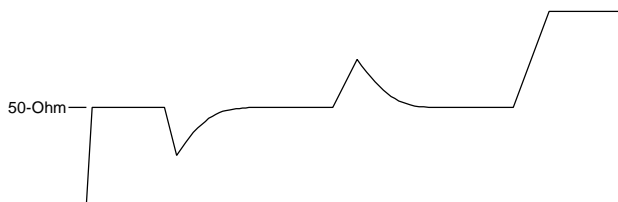
**Before starting, please check to make sure that you have all 10 pages.**

<b>1</b>		<b>30</b>
<b>2</b>		<b>20</b>
<b>3</b>		<b>20</b>
<b>4</b>		<b>15</b>
<b>5</b>		<b>15</b>
<b>Total</b>		<b>100</b>

**Problem 1: Short Answer (30 Points: 10 questions, 3 points each)**

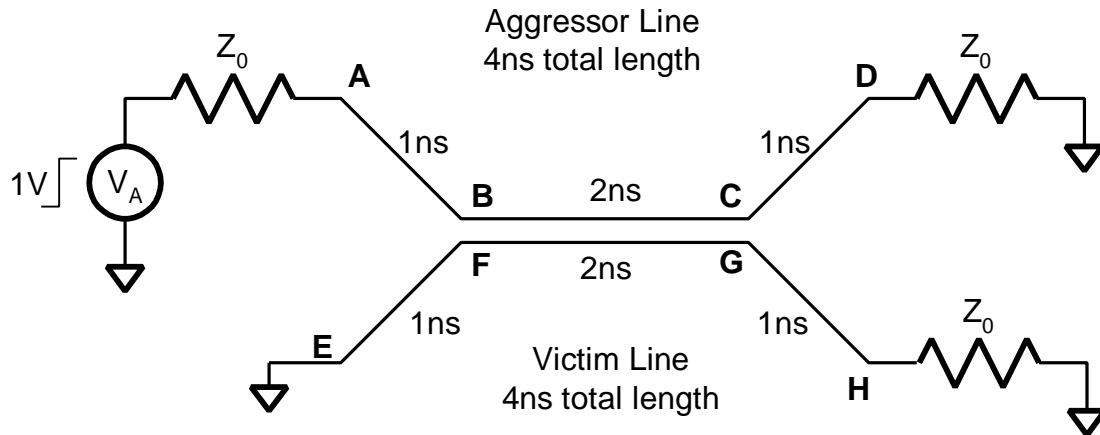
- A. Suppose you have a *parallel plate* transmission line (a pair of flat conductors that are wide enough that you can ignore the fringing fields – their capacitance is well approximated by the parallel plate component) with a characteristic impedance of  $100\Omega$  and a velocity of  $1.5 \times 10^8$  m/s. If you double the spacing between the two lines. What happens to the impedance of the line?
- B. For the transmission line of (A), what happens to the impedance when the width of the lines is doubled?
- C. Consider a 2Gb/s signaling system. At 1GHz the transmission line used by the system has an attenuation of  $A=0.7$ . There is essentially no attenuation,  $A=1$ , at DC. Without equalization, what will the vertical eye opening be for a worst case bit pattern. Express your answer as a fraction of signal swing.
- D. In an on-chip RC transmission line using optimal repeater spacing, if the capacitance per unit length of the wire is halved (and the repeater spacing adjusted to still be optimal), by what amount and in which direction does the delay per unit length change?
- E. You wish to connect a  $50\Omega$  transmission line to a  $100\Omega$  transmission line. Sketch a resistor network that you could place between the two lines that will allow waves to propagate from one line to the other in just one direction (from the  $50\Omega$  line to the  $100\Omega$  line) without reflections.

- F. You have designed a signaling system with a BER of  $10^{-12}$ . If the Gaussian noise sources in this system are halved while everything else is held constant what will the new BER be?
- G. You are designing a backplane bus. The unloaded bus and stub traces have a capacitance of  $100\text{pF/m}$  and an inductance of  $300\text{nH/m}$  ( $Z_0 = 55\Omega$ ,  $v=1.8 \times 10^8 \text{ m/s}$ ). The spacing between stubs is  $4\text{cm}$  and the stubs are  $10\text{cm}$  long and terminated in a  $10\text{pF}$  load. What is the effective impedance of the loaded bus traces?
- H. What is the fastest rise time that you can safely transmit over the backplane bus of (G)?
- I. You transmit a  $1\text{V}$  step into a  $10\text{m}$  cable that has a signal conductor with an inductance of  $200\text{nH/m}$  and a return conductor with an inductance of  $100\text{nH/m}$ . Just after the transition at the source, what is the voltage difference between the two ends of the return conductor?
- J. A TDR of a transmission line shows the following waveform. Sketch qualitatively (no component values) a possible model for the line.



## Problem 2: Transmission Lines (20 Points)

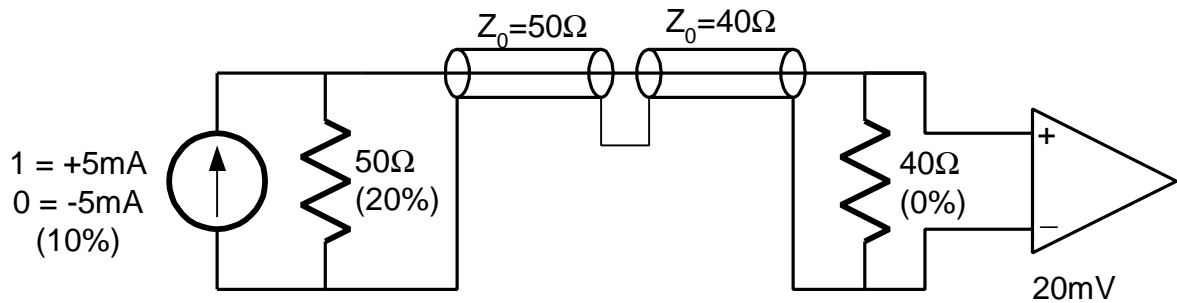
Consider the pair of coupled transmission lines shown below. The coupled section of each line has a near-end crosstalk coefficient  $k_{rx}$  of 0.1 and a far-end crosstalk coefficient,  $k_{fx}$  of 0. The aggressor line is driven directly by a 1V step source with a rise time of 100ps. The far end of the aggressor is terminated in a matched impedance. The victim line is shorted to the ground plane at the source end and terminated with a matched impedance at the far end. Note that the 'ground' symbol here denotes a local connection to the shared ground plane, not a single-point ground.



Using this information, sketch and dimension the voltage waveform at the far-end of the victim line (point H). You may ignore any effects that lead to waves with less than 10mV amplitude.

### Problem 3: Signaling and Noise Analysis (20 points total)

Consider the bipolar current-mode signaling system shown below. At nominal levels, a logic “1” is represented with 5mA of current drive and a logic 0 is represented with -5mA of drive. The actual transmitter levels are within 10% of these nominal levels. The line is terminated at both ends into matched impedances with 20% tolerance at the source end and a perfect match<sup>1</sup> at the receiver. The line itself has a 20% impedance discontinuity (from 50Ω to 40Ω – note the length of these segments does not matter). The receiver has a combined sensitivity and offset voltage of 20mV. In addition, there is a 20mV Gaussian noise source (not shown) adding noise to the line.



- A. (10 points) List all of the relevant noise sources for this system and compute the net noise margin.  
(Hint: you may ignore all forms of crosstalk and may ignore all reflections after the second bounce).

- B. (5 points) Compute the BER for this signaling system.

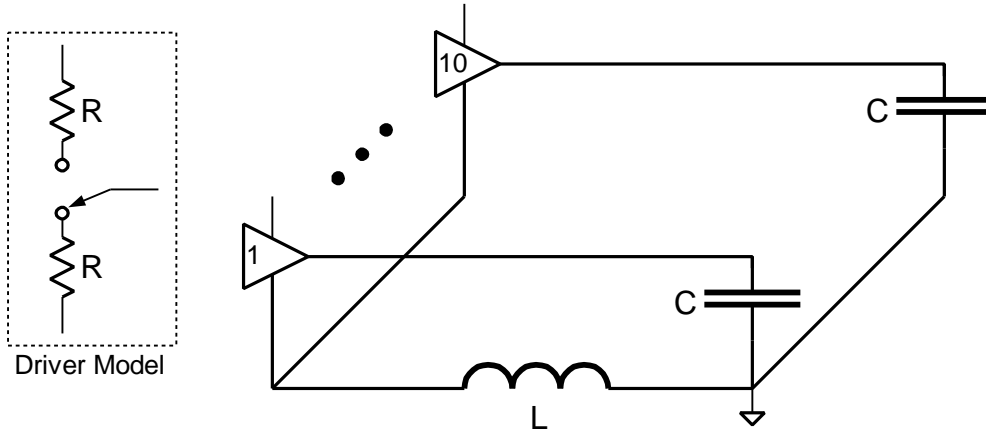
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<sup>1</sup> This is not realistic but it simplifies the problem.

- C. (5 points) Suppose 50mV of hysteresis is added to the receiver. That is its decision point rather than being at 0V is +50mV when the output is low and -50mV when the output is high. What are the values of the net noise margin and the BER with this hysteresis?

### Problem 4: Signaling over Lumped Loads (15 Points Total)

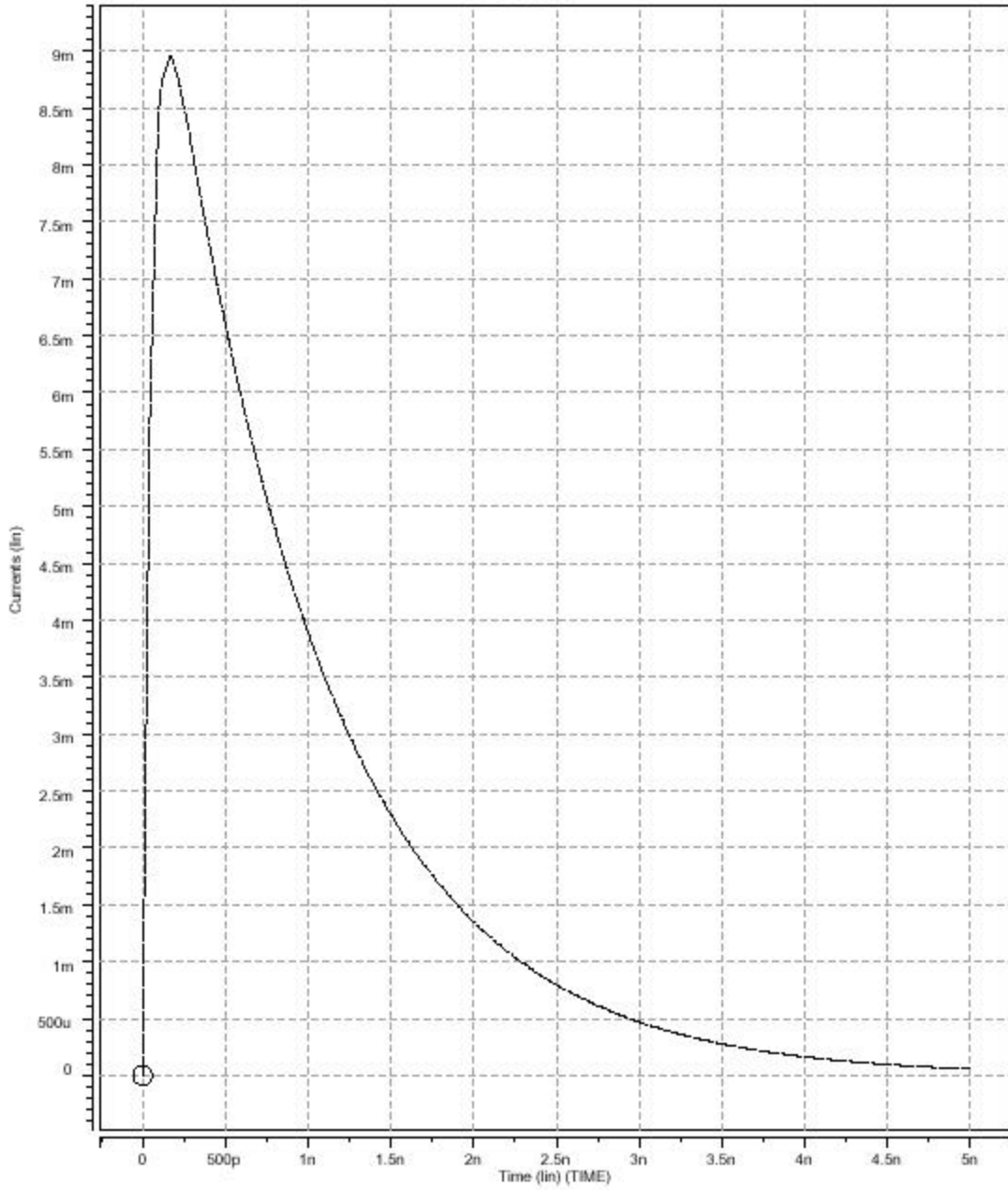
Consider the system shown below for signaling over a medium that is modeled as a lumped capacitor. Ten drivers share a single ground return pin with inductance  $L = 5\text{nH}$ . Each is loaded with a  $C = 10\text{pF}$  capacitor.



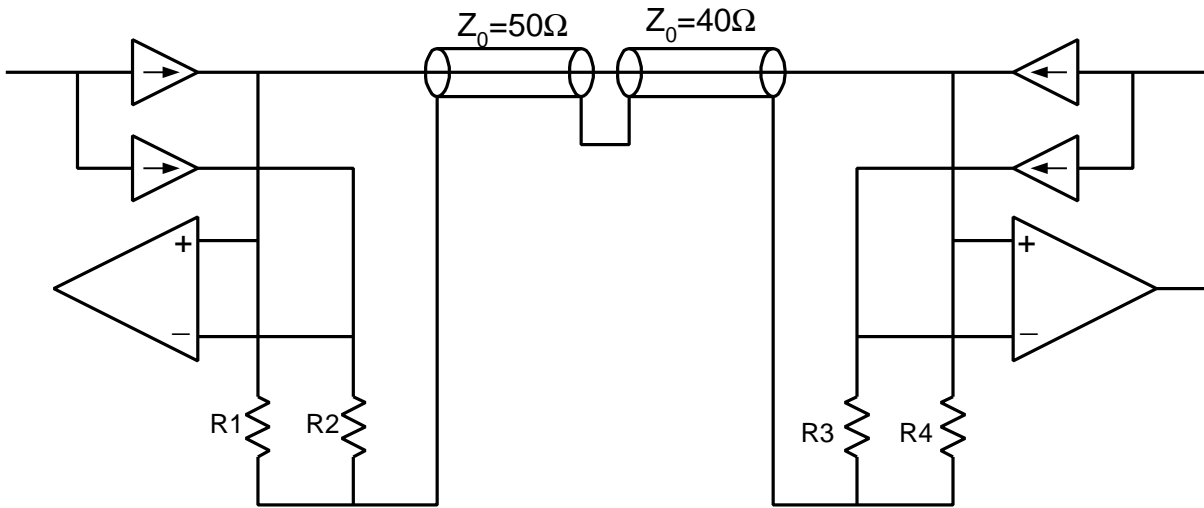
- A. Suppose we use a driver that is accurately modeled as a switch and two resistors with value  $R = 100\Omega$  as shown in the box at the left of the figure. Consider the case where nine of the drivers are initially high with outputs at 1V while the tenth driver has a low 0V output. What happens to the voltage on the output of the tenth output when the nine high outputs simultaneously switch from the high resistor to the low resistor? Sketch the resulting waveform. (Hint: the current waveform from this driver in the configuration shown above is plotted on page 9).
- B. Suppose instead of the resistor and switch driver that you can substitute a driver that produces an arbitrary current waveform. What is the optimum driver current waveform that minimizes noise on the unswitched output while still switching within 2ns? Sketch the waveform.

- C. What is the noise on the unswitched output when nine drivers simultaneously switch low using the current profile from (B)?

\* Irc i/o circuit



### Problem 5: Advanced Signaling (15 Points)



The figure above shows a simultaneous bidirectional signaling system that shares all parameters (transmit levels  $\pm 5\text{mA}$  (10%), receiver offset+sensitivity =  $20\text{mV}$ , and resistor tolerances 20%) with the signaling system of Problem 3. For simplicity, the replica current drivers here are full-scale. That is each of the four drivers in the figure above drives a nominal value of  $+5\text{mA}$  for a 1 and  $-5\text{mA}$  for a 0. Also for simplicity, assume that resistors R2 and R4 are exact while R1 and R3 have a tolerance of 20%.

- A. What are the proper nominal values for resistors R1 through R4?
  
- B. Compared to the system of problem 3, what new noise sources and modes must this system contend with? List the sources and give the magnitude of each source. Consider just noise sources affecting the signal traveling from left to right.
  
- C. What is the net noise margin of this system for the signal traveling from left to right?