EE273 Digital Systems Engineering
Course Policy

Room: Skilling Auditorium
MW 11:00 to 12:15

Problem Sessions:
TBD

Instructor: William J. Dally
billd@csl.stanford.edu
Gates Room 301
(650)725-8945
Hours: MW 10:00 to 11:00 (except as noted – see announcements)

TAs: Patrick Chiang
pchiang@leland.stanford.edu
Hours: TBD

Greg Larchev
gregl@stanford.edu
Hours: TBD

Support: Pamela Elliott
pamela@csl.stanford.edu
Gates 303
(650)725-3726

On-Line Info: available via http://eeclass.stanford.edu/ee273/

Goal

The course is intended to give the student an understanding of the fundamental electrical issues involved in the design of high-performance digital systems and a mastery of the basic techniques and methods used to deal with these issues. Issues will be introduced in the areas of signaling, timing, synchronization, noise-management, and power distribution. In each area, the fundamental problems will be introduced and engineering solutions to these problems discussed. In the area of signaling, for example, the problem of signaling over transmission lines will be introduced and incident-wave signaling methods will be described.

Assignments

There will be six weekly homework assignments and a class project. All assignments will be posted on the course web page. The project will involve developing a solution to a significant problem related to the course material.

Late Assignments

Homework is due at the **beginning** of class on the due date. There will be no credit given for late homework assignments. All SITN students must turn in their assignments at the same time as on-campus students. There is no delay for remote SITN students taking the course via Stanford on-line. The course is not offered via TVI.

Collaboration

Collaboration on homework assignments is encouraged subject to the following guidelines:

1. No more than three people can collaborate on a homework solution.
2. Groups of people working together should submit a single homework solution for the group.
3. Any assistance received in the solution of a homework assignment should be acknowledged in writing on the homework assignment.

Exams

There will be a Midterm exam and a Final exam. The Midterm will be held in the evening on **Monday February 12.** . There will be class on the day of the Midterm but there will be no homework assignment that week. The midterm will cover material up through that presented on February 7. The Final exam will be held on **Friday March 23** from 8:30AM to 10:30AM (two hours) and will be comprehensive. Local SITN students must come to Stanford to take the Midterm and the Final. Please plan to attend both the midterm and final and organize your schedule accordingly. Alternative exam times will be made available only under extreme circumstances. Remote SITN students must observe the time limits for the midterm and final and must submit their completed exams no later than the day after the on-campus exam. No credit will be given for late exams. Requests to re-grade exams must be submitted **in writing** within one week after the exams are graded. An exam submitted for re-grading may have all questions re-graded, not just the one requested.

Problem Sessions

The TAs will hold weekly problem sessions on Fridays. This session will be used for review sessions for the Midterm and the Final and for a demonstration of transmission line operation on February 2.

Grading

Homework Assignments	20%
Midterm	25%
Final	35%
Project	20%

Text

Dally and Poulton
Digital Systems Engineering
Cambridge University Press, 1998

Prerequisites

EE113 or equivalent, EE121 or equivalent. You must understand ‘basic’ circuit design and logic design concepts.