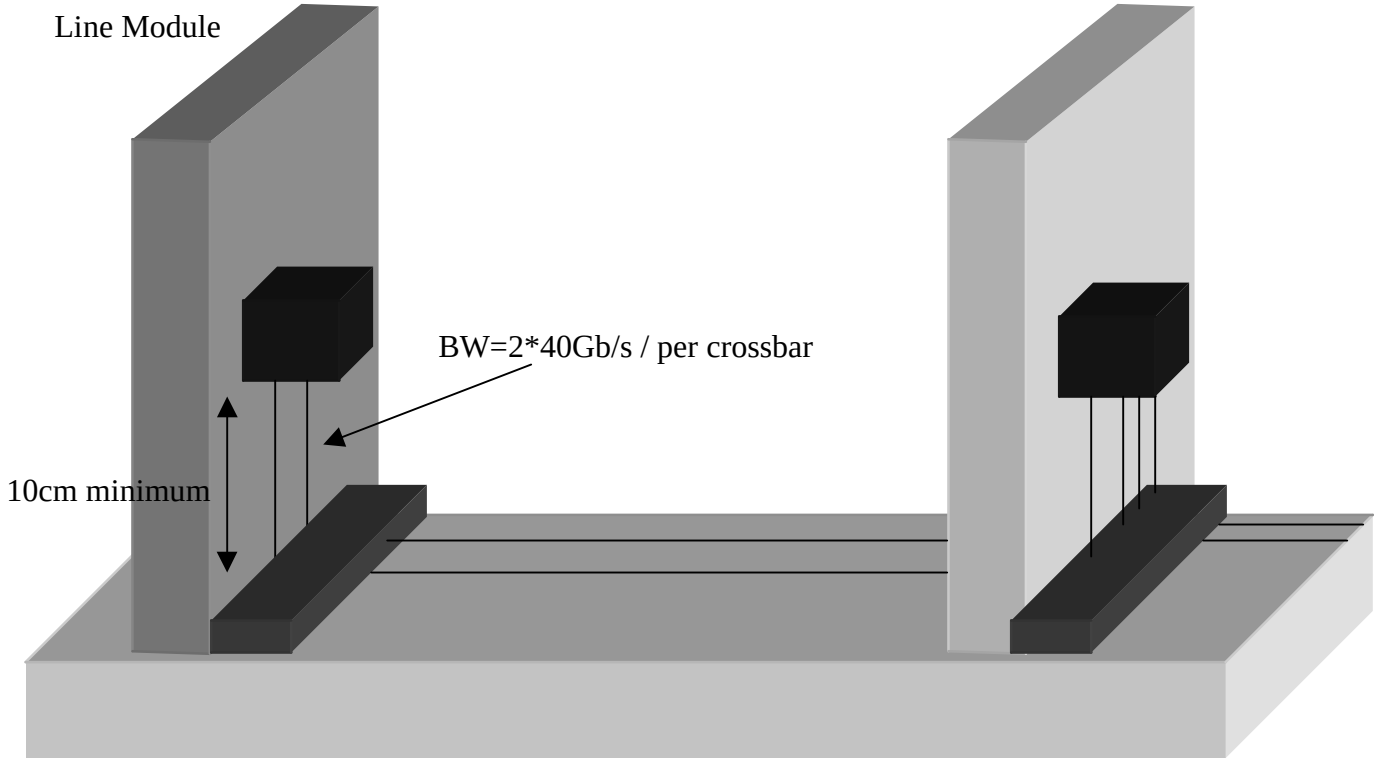
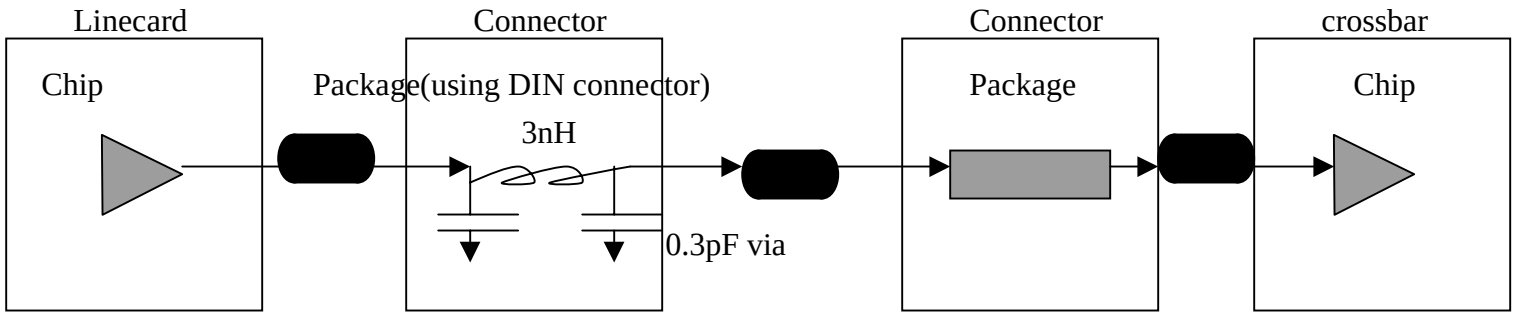
This project is to design the physical layer for a terabit IP router. Each line module is 20cm by 40cm by 3cm. The 20cm or the 40cm edge can be placed into the backplane. Assume line cards can be placed directly side by side. Each IC chip must be minimum 10cm away from the edge of the line card. i.e. the distance from one IC chip to another IC chip on abutting line cards, is 10cm + 3cm + 10cm. One particular illustration is that below, showing one crossbar, and one line card.





Basic Connectors—allow up to 1 signal conductor for each 1mm of board edge. Cost is $0.10/signal conductor. The connector is modeled as a lumped 3nH inductor with a coupling coefficient of 0.1 to the two adjacent pins.

Dense Connectors: These DIN-style pin-in-socket connectors are built on a 2mm grid. You may use connectors with either four or six rows of contacts. The equivant circuit is the same as the basic connector. You are free to place ground and power at positions of your choice, and may use extra ground connections as shielding between active pins. Cost per mated contact for this style of connector is $0.15.

You may use other/better connectors if you find the specs for them.

Chips—you have a total of 768 pins. Some of these signal pins have to be at the lower rate(64 signals at 622Mb/s). These 64 pins at 622Mb/s(OC-12) are parallel to serial converted to 40Gb/s(OC-768). Also need to provision for pwer and ground pins.

For the 1cm transmission line inside the package, just assume that the signal propagates along it at half the free space speed of light(~150nm/ns). For the connector, assume lumped 3nH inductor, with vias on both sides.

Jitter and Skew analysis—short list of possible timing conventions:

- Sychronous timing
- Pipelined timing
- Bundled closed-loop timing
- Per-line closed-loop timing
- Etc

Transmission Lines in HSPICE

We recommend you to use W elements for the transmission lines. Refer to chapter 21, p. 72 of the HSPICE manual. You need to design a RLGCfile(chapter 21, p. 80).

Here are some brief hints for building R, Rs(skin effect), G and Gd(dielectric loss) matrix.

- R: diagonal matrix(off diagonal values=Rij=0, I=J) with Rii=Rdc for each line. You may scale the value from a known value of Rdc=7 ? /m (5-mil copper stripline).
- Rs: diagonal matrix (off diagonal values=0), and the values ofor diagonal elements should be $R_{S,II}$ =R(f)/sqrt(f) = Rdc/sqrt(fs), where fs is the skin depth frequency
- G: since the conductorance of the line at DC is small, just put o's for all elements.
- Gd: $_{G\,D,\,I\,J}$ = G(f)/f=2*pi*tan(deltaD)*Cij, for all I and J

Reference: http://www.ece.orst.edu/~moon/hspice98/files/chapter_21.pdf

Here are some addendums to this year's project. Many of these are related to the project that was given last year.

Signaling rate: This is the key parameter that will drive both the cost, and all other design decisions in your system. Because it depends on line length, signaling convention, and timing convention, it cannot be finalized until you have completed your design. However, a preliminary signaling rate needs to be one of the first things you choose in coming up with the design. Iterations may be needed if you can't achieve this initial rate. In general, those with higher signaling rates (multiGb/s) are going to have the lowest cost solutions. Rates of less than 1Gb/s are too slow to be competitive.

You need to show the board 'stackup'(cross-section of the PCB. This determines your attenuation, crosstalk, impedance, etc.

Signaling Convention: Describe your convention clearly with a schematic of a link showing the transmitter, terminations, and receiver as well as any relevant in-link elements. Make sure you give all of the relevant parameters like current drive, rise-time, etc.

Noise Budgets: At a minimum your noise budget must consider frequency-dependent attenuation (depends on line geometry and length), crosstalk(depends on line geometry), ISI (depends on line discontinuities and termination mismatch), transmitter offset, receiver offset, Gaussian noise due to the terminator, and Gaussian noise due to unaccounted for crosstalk.

Timing Convention: Carefully explain where you get the sample clock for each received signal and how you guarantee that this clock is centered on the eye. State your requirements for matching of line lengths. Identify and quantify your sources of skew and jitter.

Timing Budgets: These should include rise-time, aperture, and jitter. Note that you need not have a 'flat spot' in the eye as wide as the aperture. As long as the signal magnitude is above threshold during the entire aperture time the signal will be correctly detected.

Return Pins: If you are operating a single-ended (not differential) signaling system. Make sure you adequately provision return pins on the chips and connector. Two returns pins will probably not be adequate for 32 signal pins. Also make sure to include the signal return crosstalk due to the sharing of these pins in your noise budget.

Keep your rise times as slow as possible to avoid exciting parasitics. As a rule of thumb, rise time should be between 30%-90%.

You may decide to use microstripguides(signal traces on board surface). Although it may save money, make sure you account for far end crosstalk.