EE273 Digital Systems Engineering
Class Schedule

The following is a tentative schedule for EE273 Winter Quarter 2000/2001. The reading assignment lists the reading that is expected to be assigned during each lecture. It should be completed before the start of the next lecture. The assignment gives a tentative outline of the problem set that is assigned during each Wednesday lecture (except as noted). For details on each assignment see the course web page. Each assignment is due at the start of the following Wednesday lecture.

No	Date	Topic	Reading	Assignment
1	10-Jan	Introduction to Digital Systems Engineering: overview of signaling, power distribution, timing, and noise issues. Simple transmission lines.	Chapter 1, Sections 3.1 through 3.3.3	PS1: 3-2, 3-10
	15-Jan	Martin Luther King Day - No Class		
2	17-Jan	Electrical models of wires. R,L,C, and G of wires. Incremental model. Propagation constant. Lossless transmission line model. Derivation of Telegrapher's equation.	Sections 3.3.4 and 3.3.5	PS2: 3-8, 3-11, 3-16 (new waveform)
3	22-Jan	Lossy lines. Skin effect resistance and dielectric absorption.	Sections 3.4, 3.6, and 3.7	
4	24-Jan	Multidrop buses. Balanced lines. Common and differential mode analysis. Time domain reflectometry. Wrapup of wires.	6.1 through 6.3	PS3: TBD (signaling)
5	29-Jan	Noise: Overview of noise sources. Power supply noise. Crosstalk - capacitive lines - coupled transmission lines - even and odd mode deriviation - signal return crosstalk.	6.4 through 6.6	
6	31-Jan	More on noise: intersymbol interference, alpha particles, thermal and shot noise, parameter variations. Managing noise. Noise budgets and BER.	7.1 and 7.3	PS4: TBD (noise)
7	5-Feb	Signaling: A quick comparison. Transmission modes, receiver operation - references and noise cancellation, termination methods. Differential signaling.	7.4 and 7.5	
8	7-Feb	More signaling: Signaling over capacitive lines. Signaling over inductive lines. Signal encoding.	8.1 through 8.4	No PS this week, study for midterm
DEMO	9-Feb	Demonstration of transmission lines.		
9	12-Feb	Advanced signaling. Simultaneous bidirectional signaling. Driving lossy RC lines. Equalization for lossy LRC lines. DC balanced codes.	Chapter 5	
Midterm	12-Feb	Midterm in the evening, location TBD		
10	14-Feb	Power distribution. Load currents. Supply networks. Bypass capacitors. Local regulation.		Project assigned PS5: 5-12 (spice your solution - see notes)
	19-Feb	President's Day - No Class		
11	21-Feb	On-chip power distribution	9.1 through 9.5	PS6: TBD (timing+sync)
12	26-Feb	Timing: Signals, values, and events. Clock domains. Timing uncertainty: skew and jitter. Synchronous timing and pipeline timing conventions.	9.6.1 through 9.6.5	

13	28-Feb	Closed-loop timing: Measuring and canceling skew. A simple timing loop. Timing loop components. Bundled closed-loop timing. Per-line closed-loop timing.	9.7	No PS this week, work on the project
14	5-Mar	Clock distribution: off-chip distribution: clock trees, phase-locked distribution, salphasic distribution. On-chip distribution: trees, meshes, jitter calculations.	10.1 and 10.2	
15	7-Mar	The synchronization problem: why synchronize, metastability and synchronization failure, calculating failure probability, common synchronizer pitfalls, synchronization hierarchy.	10.3	Project due
16	12-Mar	Synchronizer design: brute-force synchronizer; mesochronous syncrhonizers: two-register synchronizer, FIFO synchronizer; plesiochronous synchronization, dealing with data-rate mismatch, arbitrary periodic synchronization, the clock predictor.		
17	14-Mar	Guest lecture TBD		
FINAL	23-Mar	8:30AM to 10:30AM (two hours) location TBD		