

EE273 Digital Systems Engineering Class Project

Assigned: 2/14/00

Final Project Report due: 3/7/00

Overview:

Your task is to design a signaling system that connects up to 16 line modules in a high-speed router to a pair of central crossbar switches.

1. Each of the 16 line modules is physically 20cm by 40cm by 3cm.
2. Each line module requires an output channel to each crossbar with a bandwidth of 40Gb/s and an input channel from each crossbar with a bandwidth of 40Gb/s.
3. There are two crossbars (one *working* and one *protection*) each of which require a bandwidth of 40Gb/s from each line module and 40Gb/s to each line module.
4. Each crossbar is bit sliced so that it is composed of two modules – for a total of four crossbar modules in the system.
5. Each crossbar module has the same dimensions as a line module.

You are to perform the system-level electrical design of the interconnect that connects the 16 line modules to the four crossbar modules. Your design should include the following elements:

1. **Physical layout:** how the line modules and crossbar modules are arranged in space and what connectors, backplanes, and cables are used to connect them.
2. **Signaling convention:** How symbols are encoded into voltage or current, how the line is driven, terminated, and received.
3. **Timing convention:** How events are discriminated in your system, how clocks are distributed, recovered, and/or generated.
4. **Specification of Transmission Lines:** For backplanes, this includes the materials and geometry: line-widths and spacing, hole-sizes, and stackups. For cables, this includes the geometry, conductor diameter, and materials. For any connectors, specify a part number and key electrical properties.
5. **Specification of Driver, Receiver, and Timing Circuits:** As part of your signaling and timing conventions describe at a high level how these circuits operate. You will also need to develop a high-level model of the driver circuits to complete your SPICE simulation below.
6. **(Optional) Key Circuits:** You may at your option design key driver, receiver, and timing circuits. Assume you have a generic 0.13um 1.2V CMOS technology available. This is not required but will receive extra credit if included.

To validate and evaluate your design you must perform the following analyses on it:

1. **Noise Budget:** Calculate all contributions to noise and interference, compute the net noise margin, VSNR, and BER.
2. **Timing Budget:** Calculate all contributions to timing uncertainty and compute the net timing margin.
3. **SPICE Simulation of Channel:** Build an accurate SPICE model of your channel including the driver, transmission lines, connectors, terminations, and receiver. Characterize this line with a simulated TDR and TDT response. Simulate your timing and signaling conventions on this channel using a short pseudo-random sequence and an isolated “1” and “0” to generate an eye diagram. Compare the simulated eye opening with your computed voltage and timing margins. (Optional) Simulate the frequency response of your lines giving S_{11} and S_{12} parameter.

4. **Cost:** Estimate the cost of your system including printed circuit boards, cables, connectors, and any driver/receiver chips required.

Grading:

Your project will be graded according to the following criteria:

1. Completeness of design.
2. Robustness of design.
3. Creativity and elegance of design (style points).
4. Completeness of analysis.
5. Cost.

Building Blocks:

You are to realize your interconnect with the blocks listed below. You are also encouraged to research the availability of other building blocks on the web – inform the course staff if you are using building blocks not listed here.

1. Basic Circuit boards – assume plain FR4 dielectric ($\tan\delta = 0.03$), eight layers, minimum conductor width of 5mils, maximum hole aspect ratio of 10. You are responsible for specifying the stackup, conductor geometry, spacing, and other design rules to optimize attenuation and crosstalk. Given your design, you will need to develop a SPICE model of your board traces. Board cost is $\$0.10/\text{cm}^2$.
2. High-Performance Circuit Boards – with low loss dielectrics ($\tan\delta = 0.005$), more layers, and/or finer line width. Board cost varies from $\$1.00/\text{cm}^2$ up.
3. Backplane Connectors – We suggest you look at AMP HS3, Teradyne VHSD, or the recently announced Teradyne GXC. Get cost and electrical models from manufacturer web page.
4. Cable Connectors – Get cost and electrical models from manufacturers web pages.
5. Cables – Get number of conductors, electrical properties, and cost from manufacturers web pages.
6. Optical links – like the Infineon PAROLI. These are very expensive.
7. Crystal oscillators – 20ppm accuracy, 20ps p-p jitter, \$5, nominal frequency between 1MHz and 300MHz.
8. Voltage-controlled crystal oscillators – as above but voltage control of frequency with range 1% of nominal frequency.
9. Chips – you will need to use chips to drive and receive the signals in your interconnect. Each chip may have up to 768 total pins (this includes both power and signal pins) in a 1mm BGA pattern with the six outer rows populated. Chips cost \$10 plus \$0.05/pin. You will also be charged \$20/W for power. If you chose a wire bond package, chip pins each include a 1pF ESD device, a 3nH bond wire, a 1cm trace of transmission line on the package, a 1nH ball, and 0.3pF of via capacitance. If you opt for a more expensive “flip-chip” package (cost is \$30 plus \$0.10/pin) chip pins include an 0.5pF ESD device, an 0.2nH ball, a 1cm trace of transmission line, a 0.5nH ball, and 0.3pF of via capacitance.

On your chips you can use the following modules:

- 9.1. Current-mode drivers with drive of up to 20mA and rise/fall time as low as 50ps. Current drive will be within 5% of the specified value. You may specify different numbers for drive and rise/fall time.
- 9.2. Voltage-mode drivers with an output impedance as low as 10-Ohms (you may specify a different impedance) will swing between two power supplies. Voltage accuracy is set by noise on the power supplies. Rise/fall times may be as low as 50ps. Actual output impedance is within +/-20% of the specified value.
- 9.3. Controlled-output-impedance driver: This cell is a voltage driver cell with paralleled output driver transistor pairs. By setting an associated control register you can turn off one or more of the pairs to adjust the output resistance of the driver in 5% increments. Swing and supply tolerances are as in the voltage-mode driver. If you use this type of driver you must include a method for determining the actual output impedance presented by the drivers on each chip and

- setting it to match your system requirements. Process variations are assumed to give you a +/- 50% chip to chip variation in resistance from nominal for a given register setting in production parts. Within a single chip variation in resistance for a given register setting is less than 2%.
- 9.4. Termination resistors matched to within 20% of a value you specify.
 - 9.5. Programmable termination resistor: Like the controlled-output-impedance driver this is a programmable resistor constructed from a parallel combination of transistors. Setting a control register allows you to control the impedance of the resistor in 5% increments. If you use this resistor, you must include a method for setting it. As with the drivers, process variations will give a +/- 50% chip to chip variation in resistance from nominal for a given register setting in production parts. Within a single chip variation in resistance for a given register setting is less than 2%.
 - 9.6. Clocked receivers (differential) with a sensitivity of 10mV, a maximum offset of +/-40mV, and an aperture time of 20ps. You can reduce the offset using an offset calibration method if you describe in your report how this is accomplished. Input capacitance is 100fF per receiver.
 - 9.7. Unclocked receivers (differential) with a gain-bandwidth product of 10GHz (you decide how to trade between gain and bandwidth) and a maximum offset of +/-40mV. As with the clocked receivers you may use offset calibration to reduce this offset if you describe how to accomplish it. Input capacitance is 100fF per receiver.
 - 9.8. Delay lines with arbitrary programmable delay and jitter equal to 5% of the overall delay. The delay of the line may be controlled either digitally or via a control voltage.
 - 9.9. On-chip VCOs with center frequency between 100MHz and 5GHz, a tuning range of up to 5:1, and jitter of 10% of the cycle time.
 - 9.10. Phase comparators with +/-10ps phase offset.
 - 9.11. Charge pumps and loop filters as described in the book. Assume they are ideal.
 - 9.12. Flip-flops with a regeneration time constant of 100ps and a delay of 500ps.
 - 9.13. Arbitrary combinational and sequential logic modules. Assume a fan-out of 4 inverter delay is 50ps.

If you need a module that is not on this list, or if you would like to change the specification of a module, please ask the course staff and we will let you know whether your request is reasonable.

What you are to do:

Start by sketching one or more overall concepts for your design. You should then do some analysis and experimentation to select your final design concept and then flesh out the details.

We strongly recommend that you visit the course staff at an early stage of your project to validate your overall design approach before you get too far along in working the details out.

Your project report should include:

1. Overall design approach – describe your overall approach to the problem include at least
 - 1.1. A narrative description of your approach
 - 1.2. A block diagram of your system showing the bus width and speed of all signals
 - 1.3. A sketch of the physical layout of your system
2. A bill of materials for your design listing all of your components and computing the cost of the system (including the charge for power).
3. Description of each transmission line
 - 3.1. Electrical model of the line
 - 3.2. Board specification and layer “stackup” for circuit boards
 - 3.3. Specification of any connectors on the line
 - 3.4. Specification of any cables
4. Details of your signaling approach including:
 - 4.1. A link diagram showing the overall arrangement of each unique type of link
 - 4.2. Number of signals on each data bus.
 - 4.3. Unidirectional vs. Bidirectional signaling.
 - 4.4. Single-ended vs. Differential signaling
 - 4.5. Number of signal levels.
 - 4.6. Signaling rate.
 - 4.7. Signaling convention (e.g., differential current-mode).
 - 4.8. Signaling details – e.g., levels, rise-time, impedances.
 - 4.9. Details of your driver, receiver, and termination circuits
5. Details of your timing and synchronization approach including:
 - 5.1. Overall timing concept (e.g., clock forwarding)
 - 5.2. Number and location of independent oscillators
 - 5.3. A description of any manual or automatic timing adjustments (control loops)
 - 5.4. Details of your timing circuits
6. A detailed analysis of your signaling convention giving a noise budget and a calculation of BER. Your analysis should consider:
 - 6.1. Transmitter offset
 - 6.2. Receiver offset and sensitivity
 - 6.3. Crosstalk (of all types depending on your stackup, design rules, and signaling convention).
 - 6.4. Inter-symbol interference (of all types depending on your design)
 - 6.5. Gaussian noise due to termination resistors, perpendicular crosstalk, and any other factors that affect your system
 - 6.6. Power supply noise
 - 6.7. Statistical noise sources
7. A detailed analysis of your timing convention giving a timing budget that includes:
 - 7.1. A list of all bounded sources of jitter
 - 7.2. A list of all statistical sources of jitter
 - 7.3. A list of cancelled and uncancelled sources of skew
8. SPICE simulations showing
 - 8.1. Operation of your link on a pseudo-random pattern and a ‘lone-pulse’ pattern – present this data as an ‘eye diagram’.
 - 8.2. TDR and TDT simulations of your transmission line including parasitics at both ends.
 - 8.3. Any other simulations that illustrate the operation of your system.
9. (Optional) Detailed Schematics of any optional circuits you have designed and SPICE simulations showing the operation of these circuits.