Problem Set 4 Solutions.

7.2

The point of the problem is to see how serious the return cross talk due to the lead inductance is and thus to highlight the advantage of differential signaling, which is immune to such cross talk. The given system parameters are repeated below:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line impedance $Z_0$</td>
<td>50 Ω</td>
</tr>
<tr>
<td>Source Resistance $R_0$</td>
<td>50 Ω</td>
</tr>
<tr>
<td>Lead inductance $L$</td>
<td>5 NH</td>
</tr>
<tr>
<td>Pin count $N$</td>
<td>32 Pins</td>
</tr>
<tr>
<td>Required data rate $TBR$</td>
<td>8 Gb/s</td>
</tr>
</tbody>
</table>

Since the parameters for the first options are already given, (16 differential channels operating at 500 Mb/s,) let’s first find the corresponding parameters for the second option. The first step is to list all the constraints and known parameters. The number of single-ended signal pins and return pins are unknown. Assuming that we want the sum of all the pins to be equal to 32, we get equation (7-2-1), where $S$ is the number of signal pins and $N$ is the number of return pins. Also, from the fact that the combined data rate should be 8 Gb/s and the fact that the rise time is half the bit-cell width, we get equation (7-2-2), where $B$ is the bit rate per channel. And from the constraint that $k_{XR}$ be smaller than 0.1, we get equation (7-2-3), which is derived from Equation (7-8) of the textbook, except that $Z_{RT}$ is changed to $(Z_{RT}/N)$ since there are $N$ ground pins. Assuming a

\[
S + N = 32 \quad \Rightarrow \quad N = 32 - S \quad (7-2-1)
\]

\[
8E9 = S \times B = S \times \frac{1}{2t_r} \quad \Rightarrow \quad \frac{1}{t_r} = \frac{16E9}{S} \quad (7-2-2)
\]

\[
k_{XR} \leq \frac{(S - 1)Z_{RT}/N}{(S - 1)Z_{RT} + N(R_0 + Z_0)} \leq 0.1 \quad (7-2-3)
\]
constant slope current ramp, $Z_{RT}$ due to the lead inductance is approximately $L / t_r$. 
Solving equation (7-2-3) with actual numbers given:

\[
\frac{(S-1) L/}{t_i} = \frac{(S-1) 16E9 L/S}{(S-1) + (32-S)(R_0+Z_0)} = \frac{(S-1) 16E9 L/S}{(S-1) + (32-S)(50+50)}
\]

\[
\Rightarrow \frac{(S-1) 80}{(S-1) + S(32-S) 100} \leq 0.1 \Rightarrow S \leq 25.09
\]

Therefore,

\[
\begin{cases}
S \leq 25 \\
N \geq 7
\end{cases} \Rightarrow \begin{cases}
B = 320 \text{Mbps/channel} \\
t_r = 1.5625 \text{ns}
\end{cases}
\]

So, the number of signal lines has increased by 9, and the required bandwidth/pin has decreased by about 1/3.

Now, let’s compare the noise margins of these two options. Since neither the voltage swing nor the current swing is given, let’s solve the margins in terms of \( \Delta I \), the current swing on the transmission line (not the swing at the current source). Notice that \( \Delta I \) is defined as the signal swing of each wire. Thus, the gross margin for option 1 is twice that

\[
\text{Gross}_1 \text{MARGIN} = \Delta I \cdot Z_0 \\
\text{Gross}_2 \text{MARGIN} = \frac{\Delta I \cdot Z_0}{2}
\]

for the option 2, since the effective signal swing is twice \( \Delta I \), the signal swing of a single line, which is the same for the two options.

Finding the net margin for option 1: (Notice that due to our assumptions, twice \( \Delta I \) is used for proportional noise while \( V_{NI} \) is the same as for the single ended case. This is not a very realistic assumption, and normally, each component of \( V_{NI} \) and \( K_N \) needs to be evaluated to yield new \( V_{NI} \) and \( K_N \). More explanation at the end of this problem.)

\[
V_{N1} = V_{NI} + K_N (2 \Delta I \cdot Z_0)
\]

\[
\Rightarrow \text{Net}_1 \text{MARGIN} = \text{Gross}_1 \text{MARGIN} - V_{N1} = \Delta I \cdot Z_0 - V_{NI} + K_N (2 \Delta I \cdot Z_0)
\]

\[
= \Delta I \cdot Z_0 (1 - 2 K_N) - V_{NI}
\]

\[
= 35 \Delta I - 20mV
\]

Now, calculating the net margin for option 2, we include the return cross talk factor. \( K_{XR} \)

\[
V_{N2} = V_{NI} + K_N (\Delta I \cdot Z_0)
\]

\[
\Rightarrow \text{Net}_2 \text{MARGIN} = \text{Gross}_2 \text{MARGIN} - V_{N2} - V_{XR}
\]

\[
= \frac{\Delta I \cdot Z_0}{2} - V_{NI} + K_N (\Delta I \cdot Z_0) - 0.1 \cdot Z_0 \cdot \Delta I
\]

\[
= \Delta I \cdot Z_0 (0.5 - K_N) - V_{NI} - 5 \Delta I
\]

\[
= 12.5 \Delta I - 20mV
\]

is approximately 0.1 since we chose \( S \) very close to the break-even point of (7-2-3).
Note that if we ignore the $V_{NI}$ term, the $(\text{Net \_margin} / \Delta I)$ term for the first option is more than twice of that for the second option.

The table below summarizes the parameters for the two options:

<table>
<thead>
<tr>
<th></th>
<th>1st Option</th>
<th>2nd Option</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Differentially Driven</td>
<td>Single Ended with multiple returns</td>
</tr>
<tr>
<td>$t_r$</td>
<td>1ns</td>
<td>1.5625ns</td>
</tr>
<tr>
<td># of channels</td>
<td>16</td>
<td>25</td>
</tr>
<tr>
<td>rate/channels</td>
<td>500Mbps</td>
<td>320Mbps</td>
</tr>
<tr>
<td>Net_Margin</td>
<td>35 $\Delta I - 20mV$</td>
<td>12.5 $\Delta I - 20mV$</td>
</tr>
</tbody>
</table>

The pros and cons for the two options are shown in the following table. Basically, the differential signaling method has all the advantages listed on page 329 of the textbook. Determining which channel is better really depends on the application at hand. Differential signaling seems to have superior noise margin as well as many advantages over single-ended signaling. However, it may be difficult to achieve 500Mbps/pin performance even with improved noise margin. It may be desirable to have a slower rise time for the constraint outside the chip.

<table>
<thead>
<tr>
<th></th>
<th>1st Option</th>
<th>2nd Option</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>no return crosstalk -&gt; independent channels</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Larger noise margin for the same $\Delta I$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Faster rise time for same effective swing</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Half the power for same effective swing</td>
<td></td>
</tr>
<tr>
<td></td>
<td>less sensitive to clock jittering</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Smaller reflection from discontinuities on the line</td>
<td></td>
</tr>
</tbody>
</table>

We have used the same $V_{NI}$ and twice the $K_N$ for the differential signaling. However, in the real-world applications, it’s important to analyze each component of the noise sources to see how they’re different in differential signaling case. The actual analysis depends on number of assumptions and environment, and an example is shown below. Assume the noise characteristics of Table 7-4 and 7-5 of page 310.

$V_{rs}$, receiver sensitivity, as well as $V_{ro}$, receiver offset, are not cancelled by driving the line differentially, and this part of $V_{NI}$ will remain the same.
Most of $V_{eo}$, external power supply noise, will be rejected, as it affects both lines equally. Only a small fraction of this noise, the part that is not rejected, will add to $V_{NI}$.

$K_{xt}$, cross talk from other signals, will be halved, assuming it affects only one line of the differential pair (the line closer to the aggressor) and not the other line.

$K_r$, reflection from previous cycle, is unchanged. It affects each line of the differential pair equally.

$K_{to}$, transmitter offset, is unchanged. It affects both lines equally, but still reduces the signal swing available.

7.5 (Note from Greg: Apparently I have initially misinterpreted this problem, and thus gave students incorrect information about it in the office hours. I will attempt to correct this mishap. I will grade the problem myself and be very generous with points – i.e., even if the answer is incorrect, but consistent with the interpretation of the problem, students will get full credit.)

The system compares the value on the line at the start of the clock cycle to the value in the middle of the clock cycle. Hysteresis is needed to add bias to evenly separate the two possibilities - for a repeated bit there is 0 difference, for a change 0->1 or 1->0 there is $\Delta V$ difference. Thus we use hysteresis to bias the decision by $\Delta V/2$, 50% hysteresis. This gives a margin of $\Delta V/2$ for both cases which is optimal.

The system rejects all voltage noise ($V_{N2}$) that is slower than the clock frequency since it is subtracted out by comparing the signal at the beginning of the cycle with the signal later in the cycle. This also accounts for any drift on the line when its floating.

Raising or lowering the hysteresis values reduces the noise margin since the two margins will no longer be balanced at $\Delta V/2$ and the BER is determined by the smaller of the two margins.

7.8

>From the table, we have $V_{ni} = 23$ mV and $K_n = 25\%$. 

If we only had proportional noise in our system, we could have a maximum of 3 signal levels (25% is the maximum number that allows 3 levels).

However, we also have fixed noise -- so we can only have 2 levels.

Then we have:

\[ 0.5V_s = 0.25V_s + 23mV \]
\[ 0.25V_s = 23mV \]
\[ V_s(\text{min}) = 92mV \]

Modified 7.3

First, consider the unipolar system.

\[ I = 30 \text{ mA} \]

Gross Margin: \[ \delta V_1 = 0.85I*50 - 1.15I*50/2 = 0.275I*50 \]

Net Margin: \[ 0.275I*50 - 30mV - 0.25I*50 = 7.5 \text{ mV} \]

VSNR = \[ 7.5 \text{ mV}/2 \text{ mV} = 3.75 \]

BER = \[ 8.84 \times 10^{-4} \]

Now, consider the bipolar system.

Gross Margin = \[ \delta V_1 = 0.85I1*50 = 0.85 \times 15 \text{ mA} \times 50 = 0.6375 \text{ V} \]

Net Margin = \[ 0.6375 \text{ V} - 30 \text{ mV} - 0.25 \times 30 \text{ mA} \times 50 = 0.2325 \text{ V} \]

VSNR = \[ 0.2325 \text{ V}/2 \text{ mV} = 116.25 \]

BER = 0 (too small to compute).