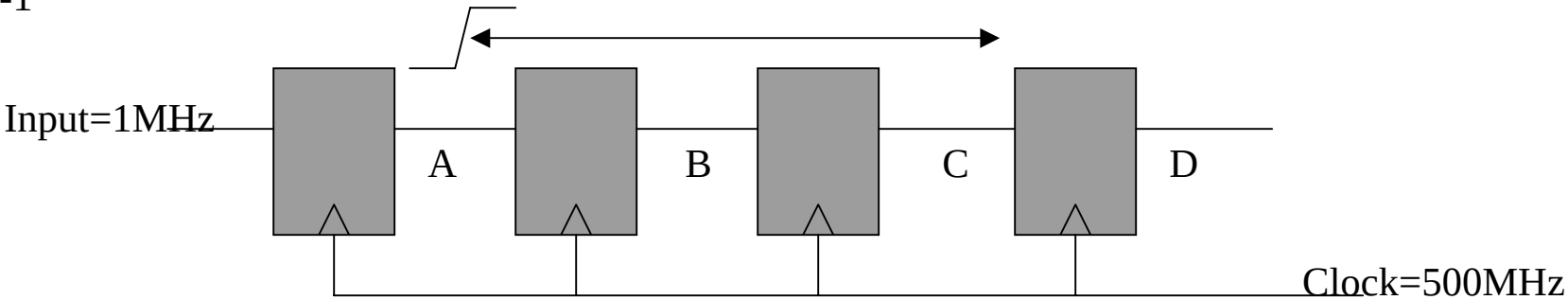
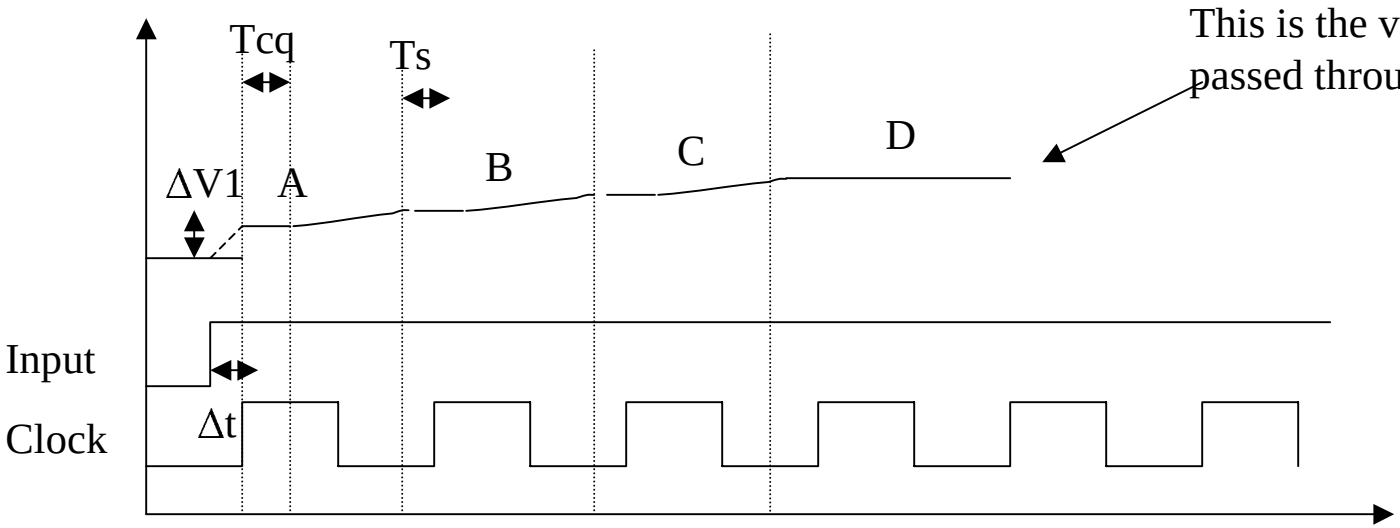
10-1



Tau[r]=200ps, Ta=Ts+Th=200ps, Tcq=500ps



This is the voltage amounts being passed through the flipflops.

Let's compute the voltage that is passed from node A to node D. If the voltage at D is not 1V unit magnitude, we expect a synchronization failure. First, the voltage Va=ΔV1=Ks* Δt, where Ks is related to aperture time Ta, Ks = 1/Ta. After a time duration of Tcq, the voltage A=ΔV1 is exponentially regenerated. However, it stops regeneration Ts before the rising edge of the clock, since this is the setup time of the latch. So, the total waiting period within one clock cycle is Tw=Tcycle – Tcq – Ts.

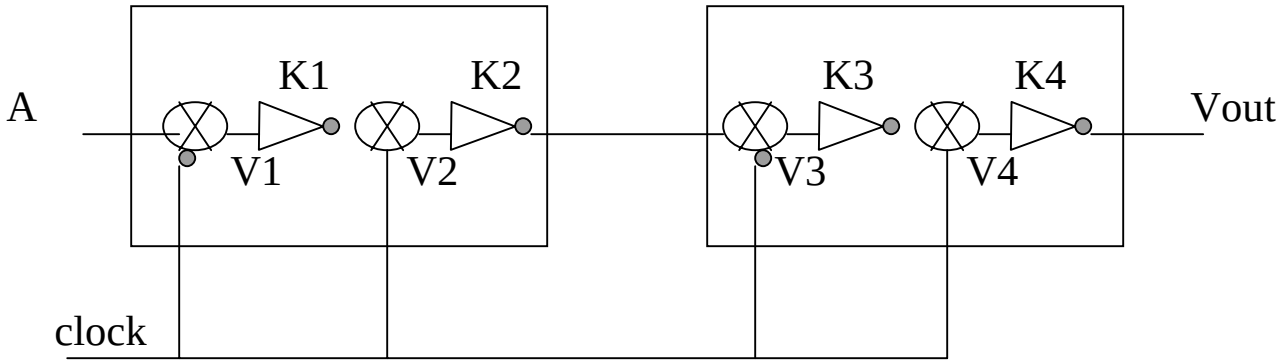
The same sort of thing occurs for node B. Node B samples the output of A after A has regenerated for Tw=Tcycle – Ts – Tcq. B now has the sampled value of A. After Tcq of the second flip-flop, Node B begins to regenerate exponentially. It also sees a waiting time of Tw=Tcycle – Ts – Tcq. This same operation also occurs for node C.

Therefore, the total waiting time of the entire synchronizer is the sum of the waiting times
→Tw(total) = 3*(Tcycle – Ts – Tcq)

→Using the equation of 10-5, Psf(Tw) = ta*fclock*exp(-Tw/tau[r]),
where ta=200ps, fclock=500MHz, Tw=4.2ns

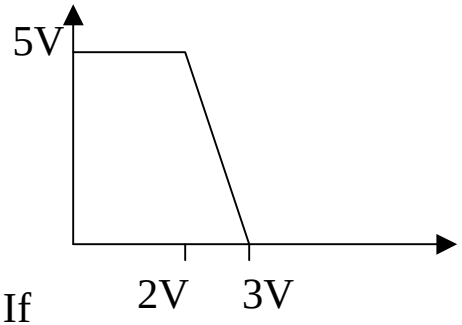
Psf(4.2ns) = 7.6e-11

Frequency of failure fsf = finput * Psf = 1e6 * 7.6e-11 = 7.6e-5.



In this scenario, no flip-flops contain any regenerative gain stages. Therefore, no matter how long the waiting time is,it is possible that the output may never switch in the right direction.

For example, suppose the Vin-Vout characteristics of each inverter looks like the scenario on the right.



Suppose now that the input A comes in, uniformly distributed such that Pa=ta*fclock. $\Delta V1$ will form at the output of inverter 1. This voltage is then gained up by the subsequent inverters to give a final voltage at Vout. If This voltage 0V < Vout < 5V, then there will be a synchronization failure. For example, suppose A is sampled such that a voltage of $\Delta V2=2.75V$ is formed on inverter 1. Calculating the gain slope of the inverter, It can be seen that for $\Delta V2=2.75V$, $\Delta V3=1.25V$, which will subsequently be enough voltage to go to full rail at Vout. (since $\Delta V3=1.25V$ will lead to $\Delta V4=5V$).

If you calculate the gain of the inverter in the high gain region, you will find that the equation for the gain region of the inverter is Vout=-5*Vin + 15.

We will now calculate the input voltage A which will cause a synchronization failure. Assume That we need V4=3V; If V4=3V, then the output Vout=0V and a valid digital signal is at the output. (This is symmetric, such that For Vout=5V, V4=2V) If V4 < 3V or V4 > 2V, there will be a synchronization failure at Vout.

Given that V4=3V, working backwards, we can find that V3=2.4V → V2=2.52V.

In other words, V2 ~ 2.5V. From equation 10-1, $\Delta V1=Ks*\Delta t$, where Ks~1/ta. The probability Of failure is essentially dependent on a low aperture time. Assuming the input is uniformly Distributed, the probability of sycrhonization failure will be 0.5*Pa=0.5*ta*fa. (There is equal probability that the input will be above the threshold 2.5V, or below the threshold)

That is, if we want Vout=0V, we need V2>=2.52V. Assuming that the distribution of the input A is uniformly distributed across the clock period, the probability of sychronization failure will be 2.52/5 * ta* fa.

Suppose now that we can put a static latch in replace of one of the dynamic latches. In this scenario, it doesn't matter where to put the static latch, as long as it doesn't replace the last latch. The reason for this is because if the static latch replaces the fourth dynamic latch, there will be No waiting time at the end to get any benefit for the exponential gain. However, if you place The static latch anywhere in the first three latches, the static latch will regenerate the input signal For half a clock cycle. I.e. the regeneration will kick in for half of a clock cycle, and give you exponential gain in any of the first three stages.