Mars Router

- 1984, 2.5μm CMOS
- 16 x16 crossbar
- Source-routed
- Bit-sliced (2-bits/chip)

Agrawal and Dally, “A Hardware Logic Simulation System”, IEEE TCAD, 1990
The Torus Routing Chip

- k-ary n-cube topology
  - 2D Torus Network
  - 8bit x 20MHz Channels
- Hardware routing
- Wormhole routing
- Virtual channels
- Fully Self-Timed Design
- Internal Crossbar Architecture

Message-Driven Processor

- Integrated Processor, RAM, Router
- Router
  - 3D dimension partitioned
  - 8b x 32MHz multiplexed bidirectional
  - virtual channels
  - synchronous
- Network Interface
  - SEND instruction
  - Create, schedule, and dispatch process on message arrival
- Row buffers

Dally et. al., “Architecture of a Message-Driven Processor”, ISCA, 1987
The J-Machine

- 1024 MDPs in a 8 x 8 x 16 grid
- Integrated 80-disk storage array
- Distributed frame buffer
Cray T3D

- 3D Torus network
- Synchronous routers
  - 1 dimension in each of 3 10K-gate ECL gate arrays
  - 150MHz x 16bit channels
- Dimension-order routing
- 4 Virtual channels/physical channel
The Reliable Router

- Fault-tolerant
  - Adaptive routing (adaptation of Duato’s algorithm)
  - Link-level retry
  - Unique token protocol
- 32bit x 200MHz channels
  - Simultaneous bidirectional signalling
  - Low latency plesiochronous synchronizers
- Optimisitic routing
Cray T3E

- 3D Torus Network
- 375MHz x 14-bit channels
- Adaptive routing using adaptation of Duato’s algorithm.
- Signal switching (for barrier network)

The Avici TSR

Up to 560 OC-48 Ports

Extensible one port at a time

Fault tolerant

QoS - RED, WFQ, CBR
at line speed