EE382C
Lecture 12

Router Datapath Components
5/10/11
Announcements

• Checkpoint 1 was due on Tuesday.
Question of the day

• On a high-radix router, is it better to:
  – Share a buffer memory across several inputs (physical channels)?
  – Have a separate buffer memory per input (physical channel)?
  – Have a separate buffer memory per input virtual channel?
Basic Router Architecture

- Router
- VC Allocator
- Switch Allocator
- Input Unit
- Output Unit
- Switch
Router Datapath Components

- **Buffers**
  - Partitioning
  - Allocation

- **Switches**
  - Bus
  - Crossbar
  - Speedup
Buffer Partitioning

Memory

Memory

Memory

Memory

Memory

Memory

Memory

Memory

Memory
Buffer Data Structures
1 - Circular Buffer

![Circular Buffer Diagram]

- Head
- Tail
- FIRST
- LAST
- Filled
- Buffer
- Memory

Buffer elements: a, b, c, d, e, f
Circular Buffer

if (~Full) {
    Mem[Tail] = new_flit ;
    Tail = (Tail == LAST) ? FIRST : Tail + 1 ;
    if (Tail == Head) Full = 1 ;
    Empty = 0 ;
}

if (~Empty) {
    flit = Mem[Head]
    Head = (Head == LAST) ? FIRST : Head + 1 ;
    if(Head == Tail) Empty = 1 ;
    Full = 0 ;
}

Can this do simultaneous insert and remove?
Buffer Data Structures
2 - Linked List
Linked List

if(Free != NULL) {
    Mem[Free] = flit ;
    if (Tail != NULL) ptr[Tail] = Free ;
    Tail = Free ;
    Free = ptr[Free] ;
    ptr[Tail] = NULL ;
    if(Head == NULL) Head = Tail ;
}


Input Buffer Allocation

• Linked list enables dynamic allocation of buffer space to individual queues (virtual channels)
• Need a policy for this allocation
• Allowing one VC to use all available storage defeats purpose of VCs
  – And can lead to deadlock
Input Buffer Allocation (2)

• Example Policy
  – N buffers total (256) [flits]
  – V virtual channels (8)
• Each VC guaranteed G = 4 buffers (VG = 32)
• Of the N-VG (224) remaining buffers, a single VC can use at most half of them (112)
• Implement policy with
  – V counters - one per VC - NV_i - number of flits in this VC’s buffer
  – 1 global counter - NU - number of flits in unallocated pool remaining
Input Buffer Allocation (3)

• Allocation to VC i allowed if:
  – NV\textsubscript{i} < 4
    • allocate reserved VC, NV\textsubscript{i}++
  – NV\textsubscript{i} >= 4 & NV\textsubscript{i} < 116 & NU < 224
    • allocate from pool, NV\textsubscript{i}++, NU++

• On Flit departure
  – if(NV\textsubscript{i} > 4) NU--
  – NV\textsubscript{i}--
Switches

• Bus switch
• Memory switch
• Crossbar
Bus Switch

Signal widths shown in phits
Bus Switch

Phit Time → Flit Time

Input Port 0: a0 a1 a2 a3 b0 b1 b2 b3 c0 c1 c2 c3
Input Port 1: f0 f1 f2 f3 g0 g1 g2 g3 h0 h1 h2 h3
Input Port 2: k0 k1 k2 k3 l0 l1 l2 l3 m0 m1 m2 m3
Input Port 3: p0 p1 p2 p3 q0 q1 q2 q3 r0 r1 r2 r3
Bus: a f k p b g l q c h m r
Output Port 0: f0 f1 f2 f3 q0 q1 q2 q3 c0 c1 c2 c3
Output Port 1: a0 a1 a2 a3 l0 l1 l2 l3 h0 h1 h2 h3
Output Port 2: p0 p1 p2 p3 g0 g1 g2 g3 m0 m1 m2 m3
Output Port 3: k0 k1 k2 k3 b0 b1 b2 b3 r0 r1 r2 r3
Phit Cycle: 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3

EE 382C - S11 - Lecture 12
Multi-Bus

Signal widths shown in phits
Crossbar

![Crossbar Diagram]

- Input Port 0 → Input Buffer → Output Port 0
- Input Port 1 → Input Buffer → Output Port 1
- Input Port 2 → Input Buffer → Output Port 2
- Input Port 3 → Input Buffer → Output Port 3
Input Speedup
Output Speedup
Input and Output Speedup
Throughput and Speedup

\[ \Theta = S_o \left( 1 - \left( \frac{k - 1}{k} \right) \frac{s_i k}{S_o} \right) \]
Network Switches
Hybrid

Input Port 1  →  Service  →  Output Port 1

Input Port 8  →  Central Buffer  →  Output Port 8

Bypass Crossbar
YARC Microarchitecture

- Regular 8x8 array of tiles
  - Easy to lay out chip
- No global arbitration
  - All decisions local
- Simple routing
- Hierarchical organization
  - Input buffers
  - Row buffers
  - Column buffers
A Closer Look at a Tile

- No global arbitration
- Non-blocking with an 8x internal speedup in subswitch
- Simple routing
  - Small 8-entry routing table per tile
  - High routing throughput for small packets
• Logic pipeline is distributed among the tiles
• 800MHz memories required flops on the input and outputs
• Each “sub-chip” floorplanning unit required flops on inputs and outputs
YARC Floorplan

- Implemented in a 90nm CMOS standard-cell ASIC technology
- 192 SerDes on the chip!
  - (64 ports x 3-bits per port)
- 6.25Gbaud data rate
- Estimated power
  - 80 W (idle)
  - 87 W (peak)
- 17mm x 17mm die
Question of the day

• On a high-radix router, is it better to:
  – Share a buffer memory across several inputs (physical channels)?
  – Have a separate buffer memory per input (physical channel)?
  – Have a separate buffer memory per input virtual channel?
Summary

• Routers built from
  – Datapath components – buffers and switches
  – Control components – allocators

• Buffers
  – Partition – global, by physical channel, by virtual channel
  – Management
    • Circular buffers
    • Linked lists

• Switches
  – Memory switches
  – Bus switches
  – Crossbars
  – Input and output speedup