

John Kim

CONTACT INFORMATION

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RESEARCH INTERESTS

Computer architecture and switching networks, more specifically interconnection networks including router microarchitecture, topology, routing, on-chip networks, and VLSI implementation; impact of evolving technologies on next-generation interconnection networks; different applications of interconnection networks (e.g. multiprocessor network, on-chip network, internet router, SAN, LAN, I/O networks) and the architectural and algorithmic issues created by their different requirements.

EDUCATION

Stanford University, Stanford, California 2002 – 2007(expected)
Ph.D. Candidate: Electrical Engineering
Advisor: Prof. William Dally
Dissertation: "High-Radix Interconnection Networks"
Cornell University, Ithaca, NY May, 1998
Master of Engineering: Electrical Engineering
Cornell University, Ithaca, NY May, 1997
Bachelor of Science: Electrical Engineering

RESEARCH EXPERIENCE

Research Assistant 2003 – present
Stanford University, Stanford, CA
Research the use of *high*-radix interconnection networks in multicomputer machines. Outlined the benefits of using high-radix routers, instead of the conventional low-radix routers, to effectively utilize the increasing pin bandwidth. Developed a scalable, complexity-effective microarchitecture for high-radix routers that provides high performance and low cost. Identified the transient load imbalance of routing in high-radix networks and the use of sequential allocation to overcome the imbalance. Proposed a cost-efficient topology for high-radix routers that reduces the number of expensive global links. Some of the research has directly impacted the network used in the Cray BlackWidow multiprocessor system, one of the first high-radix networks to be built. Currently investigating the use of on-chip networks in high-radix routers and the use of higher radix routers in on-chip networks.

Research Assistant Fall 1997 – Spring 1998
Electrical Engineering, Cornell University
Investigated through-wafer etching – etching completely through the wafer and connecting devices on both sides of the wafer. Performed various processing step by working in a clean room at the Cornell Nanofabrication Facility

TEACHING EXPERIENCE

Co-Instructor (EE382C) – Interconnection Networks Spring 2005
Stanford University
An advanced architecture course for graduate students. Prepared lectures, homeworks, and created exams and solutions. Helped design the class project on on-chip interconnection networks.

Teaching Assistant (EE282) – Computer Architecture Winter 2002
Stanford University
An introductory graduate level class on computer architectures. Held weekly office hours and helped with the development of the homeworks and the exams. Conducted televised review sessions and provided support for a course project in Verilog.

Course Lab Assistant (EE108B) – Digital Systems

Spring 2002

Stanford University

An introductory undergraduate level class on digital systems. Supported the development of the labs for this newly created undergraduate class, which involved using Verilog and FPGA. Generated lab handouts for the students.

Instructor (CMOS 105) – Introduction to CMOS

Spring & Fall 2001

San Jose City College, Department of Applied Physics

An introductory CMOS layout class for mask designers. Lectured twice per week, covering topics ranging from the basic concept of electronics and transistors to the layout of complex CMOS gate. Provided exams/quizzes to the class and supervised inclass layout labs.

INVITED TALKS

“Cost-efficient High-Radix Topology”
University of Pittsburgh, CS Seminar

October, 2006

“Interconnection Networks and High-Radix Routers”
Samsung Electronics, Kiheung, Korea

December, 2004

PUBLICATIONS

John Kim, William Dally, Dennis Abts “Flattened Butterfly : A Cost-efficient Topology for High-Radix Networks” *under submission to ISCA 2007*

John Kim, William Dally, Dennis Abts “Adaptive Routing in High-Radix Clos Network” *In the proceedings of the 2006 International Conference for High Performance Computing, Networking, Storage, and Analysis (SC’06)*, Tampa, Florida, November 2006. [Best student paper finalist]

Steve Scott, Dennis Abts, John Kim, William Dally “The BlackWidow High-Radix Clos Network” *in the proceedings of the 33rd International Symposium on Computer Architecture (ISCA-33)*, pp. 16–28, Boston, Massachusetts, June 2006.

John Kim, William Dally, Brian Towles, Amit Gupta “Microarchitecture of a High-radix Router” *in the proceedings of the 32nd International Symposium on Computer Architecture (ISCA-32)*, pp. 420–431, Madison, Wisconsin, June 2005.

John Kim, Abishek Das, “HCF: A Starvation-free Practical Algorithm for Maximizing Throughput in Input-Queued Switches”, in the *Proceedings of 2005 Workshop on High Performance Switching and Routing (HPSR)*, May 2005

John Kim, William J. Dally, Amit Gupta “Simulating High-Radix Interconnection Network” *Concurrent VLSI Architecture Technical Report*, Stanford, California, March 2005

John Kim, Chip Laub “Synthesizing Register Files”, *Intel Design and Test Technologies Conference (internal)*, 2H03, August 2003

John Kim, Earl Swartzlander, “Improving the Recursive Multiplier”, *Proc. IEEE Asilomar Conf. on Signals, Systems, and Computers*, October 2000 Pacific Grove, CA

PATENTS

John Kim, William Dally “Hierarchical Organization of a High-Radix Router” S04-286. patent pending (Stanford University)

John Kim, Rich Collins, “First-in, first-out memory system having both simultaneous and alternating data access and method thereof” Patent #6,779,055 Issued August, 2004 (Motorola)

WORK EXPERIENCE **Component Logic Designer, Sr.** 2001 – 2003
Intel, Enterprise Processor Group Santa Clara, CA
Member of the IA-64 design team. Supported the development of the synthesis methodology for the IA-64 Processors and migrated custom design units to the synthesis flow. Developed RTL strategies for appropriate logic implementations to meet timing for synthesis. Implemented several units including synthesis, back-end analysis (place & route, timing) and correlated timing and parasitics. Extended the synthesis methodology to synthesize register files.

Circuit/Logic Designer 1998 – 2000
Motorola Inc., M-Core Technology Center Austin, TX
Designed the Nexus Debug module (FIFO & instruction snoop unit) for M-Core microprocessor, including writing the microarchitecture, coding Verilog RTL, testing and verification, synthesis, and timing analysis of the module. Supported the design of the M300 microprocessor core with circuit and logic designing as well as DFT support with scan chains.

Intern Summer 1997
Samsung Electronics – System LSI Division Kiheung, Korea
Wrote behavioral description of a DSP unit as a coprocessor to the ARM using Verilog HDL. Identified strength and weakness of Human Resources in Korea compared to the US and reported to upper management.

Co-op Engineering Intern Jun 1996 – Dec 1996
IBM Microelectronics Division – Technology Simulation Department Burlington, VT
Evaluated model-to-hardware correlations for devices/circuits. Investigated the Response Surface Model of performances in circuit simulation using linear regression analysis