EE 316 Design Project

Final report

Parasitic Engineering for Double-Gate FETs

Winter 2010

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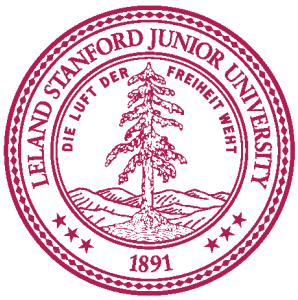

Abstract:

Extrinsic resistance due to lateral extension doping profile can become a performance-limiter in ultrathin body Double-Gate FETs (DGFET). Historically, the intrinsic gate capacitance dominates the capacitance while the channel resistance dominates the total resistance. With devices reduced to nanometer scale, parasitic capacitances and extrinsic resistances significantly affect the device delay. For a given lateral doping gradient, the extension doping needs to be offset from the gate edge by an amount called the underlap. The current drive, and hence transistor performance, is maximized when the underlap is chosen in such a way as to balance the impact of non-abrupt doping on the short channel effects and series resistance. In this report, two-dimensional device simulations are used to study and optimize the device performance in a 50nm gate length DGFET. The silicon body thickness has been optimized to reduce DIBL and R_{ON} of the device or in other words to increase the ON/OFF current ratio of the device. The spacer thickness is optimized to pick the maximum device performance by looking at the device parasitic capacitance and extrinsic resistance.

Introduction

According to the ITRS Roadmap, alternative MOSFET structures are going to be needed for scaling device beyond roughly 16nm [1]. The ultrathin body Double-Gate FET (DGFET) is one of the primary candidates for replacing conventional bulk MOSFET transistors. The DGFET has been shown to have very good electrostatic gate control over the channel, enabling gate length scaling down to 10nm [1]. In these devices, the ultrathin body, whose thickness is typically *1/3* to *1/2* of the gate length, is the key to suppressing short channel effects such as *Vt* roll-off, drain-induced barrier lowering (DIBL), and degraded sub-threshold swing. However, it introduces an extrinsic parasitic resistance, R_s, in series with the channel and the source/drain electrodes. The effective gate overdrive is reduced by an amount $I_d \times R_s$, where I_d is the drain-source current when the transistor is turned on and in saturation. This problem is quite severe in DGFET devices as the presence of two channels leads to twice the current

flowing through the series resistance as compared to MOSFET devices, leading to higher potential drop across the extrinsic resistance.

In this work, we use two-dimensional device simulations to engineer and optimize the effect of parasitic resistance and capacitance in a 50nm n-channel DGFET. Part I of this report is related to finding an optimum silicon thickness (T_{si}) for our DGFET structure. In part II, the effect on T_{spacer} on threshold voltage (V_{tsat}) and sub-threshold slope (SS) of the DGFET is investigated. In part III, an optimal T_{spacer} value to achieve the highest device performance is proposed. To do so, the delay of an inverter with fan out of one is used for modeling the delay parameters. At the end of this part, we discuss the effect of a few other parameters on the device performance such as the effect of doping gradient abruptness, spacer dielectric constant variation, and raised S/D height variations.

Part. I DGFET Schematic and structure:

Fig. 1 illustrates the structure and doping profile of our DGFET structure for three different T_{si} values. For a constant lateral doping gradient, the S/D overlap doping profiles become quite different. Electric potential profile of the channel for 5nm and 36nm DGFET structures are provided below (Fig 1b and c); the later has much higher DIBL effect and worse gate control over channel.

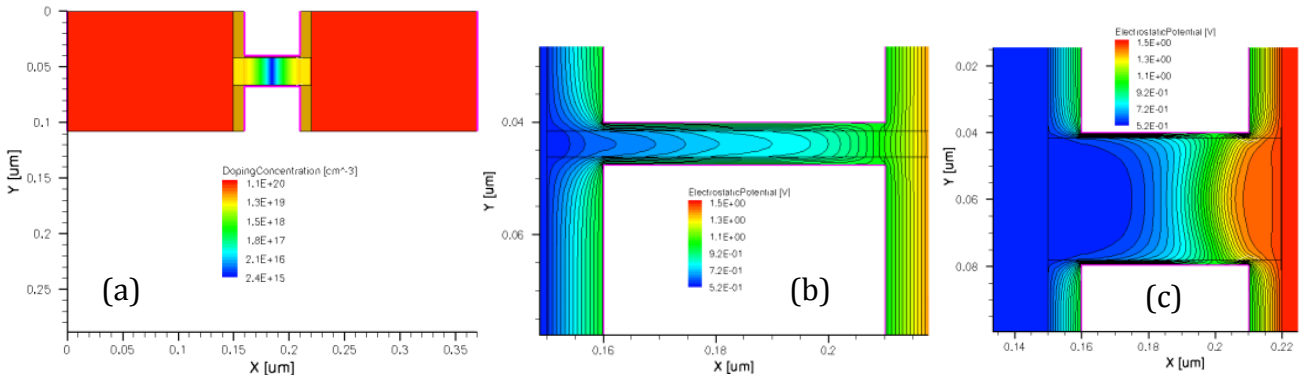

Fig.1: DGFET Structure and Doping Profile, (a) for the nominal case Tsi=24nm,

Electric potential for (b)Tsi= 5nm (c)Tsi= 36nm

To find the nominal T_{si} value, we used the following scale length equation [2]:

$$1 = \frac{\varepsilon_{Si}}{\varepsilon_{ox}}.\tan\left(\frac{\pi\, t_{ox}}{\lambda}\right)\cdot\tan\left(\frac{\pi\, t_{Si}}{\lambda}\right)$$

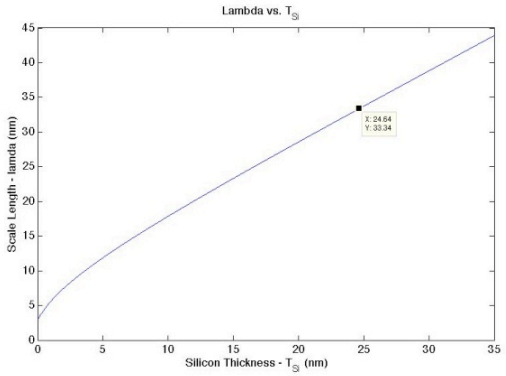

Fig 2: Scale length vs. T_{si}

Plugging in all the given values and using Lg/λ=1.5, we find the nominal λ=33.33nm and the nominal Tsi=24.64nm. Fig. 2 shows the plot of the above expression.

To find an optimal T_{si} that increases the ON/OFF currents ratio, one must consider its effect on both DIBL and R_{ON}. In order to find an optimum value for R_{ON} and DIBL, the device was simulated for various T_{si} values ranging from 5nm to 40nm. According to the explanation given in the interim report, the optimum Si thickness was determined to be roughly 18nm. Fig. 3 illustrates the results.

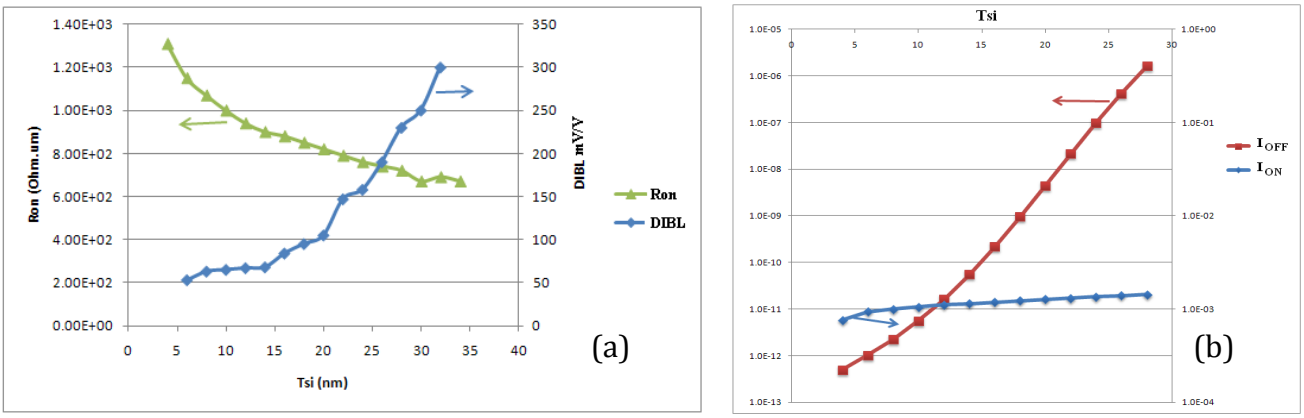

Fig 3. (a) *DIBL* and R_{ON} vs. T_{si},(b) I_{on} and I_{off} vs T_{si}

Part II. *Vt* and *SS* of the proposed DGFET as a function of T_{spacer}:

In this part, the simulation has been done for constant optimal T_{Si} =18.64nm determined in part I for several T_{spacer} values ranging from 2 to 30nm. The Id-Vg plots have been extracted for each T_{spacer} at constant $V_{DS}=V_{DD}$=1V. Vt_sats are calculated by using the constant current method at 10µA/W. The inverse subthreshold slope, SS, has been derived by looking at the minimum value of $(\partial(\log Id)/\partial Vgs)^{-1}$ of the extracted I_d-V_{gs} curves.

The induced electric field is inversely proportional to the spacer thickness. That is, as T_{spacer} increases, the induced electric field from S/D to the channel decreases. Furthermore, as T_{spacer} increases, the S/D doping profile under the gate overlap is decreased. As a result, the gate control over channel region is improved and hence DIBL is reduced, threshold voltage is increased, and the inverse sub-threshold slope is decreased. Fig 4 and 5 show the effect of the spacer thickness on *Vt* and *SS* respectively. Fig. 6 illustrates our DGFET device with different T_{spacer} values.

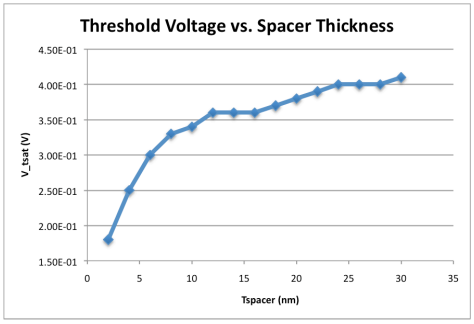

Fig 4: $V_{t\text{-}sat}$ as a function of T_{spacer}

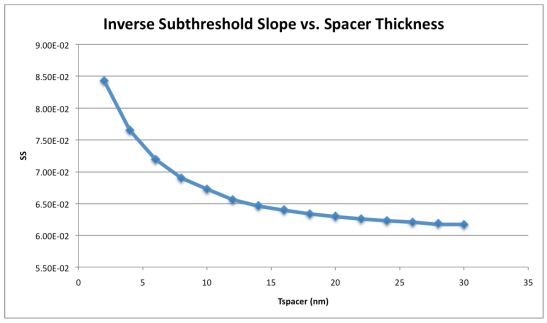

Fig 5: SS_{sat} as a function of T_{spacer}

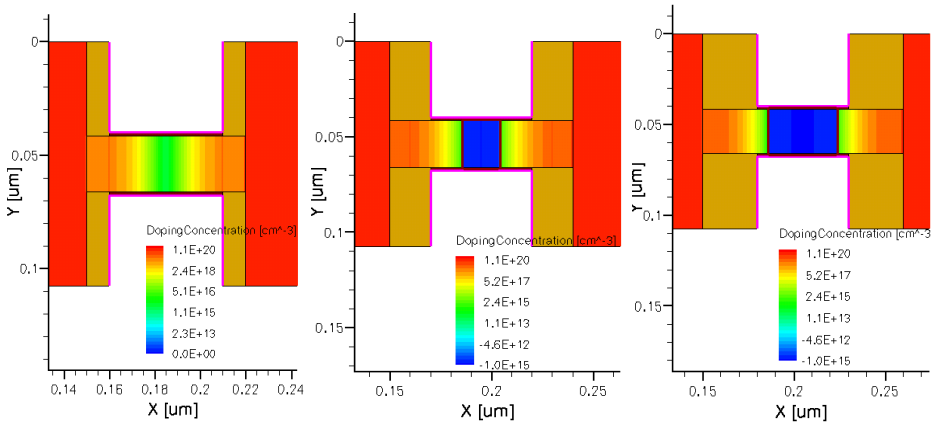

Fig 6. Simulated structure when T_{spacer} (a) 10nm, (b) 20nm, (c) 30nm

Figure 6d provides the lateral band diagram of our DGFET device for the the following four T_{spacer} values: 10nm, 16nm, 20nm, and 30nm. As T_{spacer} decreases DIBL effect increasees.

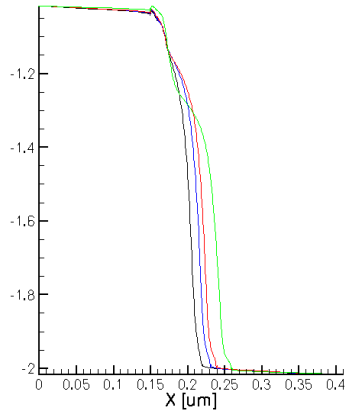

Fig 6. Lateral Band diagram: Gray: 10nm, Blue: 16nm, Red: 20nm, Green: 30nm

Part III. Circuit performance, RC Delay, as a function of Tspacer:

In this part we calculate the delay of an inverter with fan out of one. In Fig 7 we have shown a simple 2-stage inverter. For finding the delay, this definition has beei

$$\tau = \int_{V_{GS}=V_{DD}/2}^{V_{DS}=V_{DD}/2} \frac{C_{eff}}{I_{DS}(V_{GS},V_{DS})}\, dV_{DS} = \frac{C_{eff} V_{DD}}{2 I_{eff}}$$

where,

$I_{eff} = (I_H + I_L) / 2$

$I_L = I_{ds}$ *at* $(V_{gs}=V_{dd}/2,\ V_{ds}=V_{dd})$,

$I_H = I_{ds}$ *at* $(V_{gs}=V_{dd},\ V_{ds}=V_{dd}/2)$ [3].

and,

$C_{eff} = C_{in} + C_{out} + C_L$

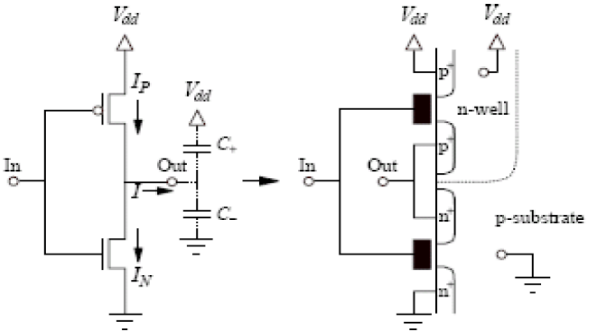

Fig 7: a simple 2-stage inverter

To calculate the worse case delay of this inverter, one should look at the situation where the effective capacitance is maximized and the effective current is minimized. We know that all the device capacitances are a function of the width of transistor. Since we only have the structure for the NMOS,

we will get all the capacitances associated with it and to get the PMOS capacitance we multiply the NMOS ones by a factor of 2 to obtain roughly the same current drive for both NMOS and PMOS. As we can see, the worst case happens when the transistors get in to the linear regime because we'll see the full intrinsic gate capacitance instead of a *2/3* factor of it. The worst case situation is when the input voltage to the first stage is *1V* and the output of this stage is at *0V* because in this case PMOS is of the second stage is ON and its NMOS counter part is OFF. In this case, the higher effective capacitance compare with when input to the first stage is *0V*.

First stage: $NMOS_{(Linear)}$ $PMOS_{(OFF)}$
Second stage: $NMOS_{(OFF)}$ $PMOS_{(Linear)}$

$$C_{in} = C_{gs\ (NMOS,\ OFF)} + 2C_{gd\ (NMOS,\ OFF)} + C_{gs\ (PMOS,\ ON)} + 2C_{gd\ (PMOS,ON)}$$
$$= C_{gs\ (NMOS,\ OFF)} + 2C_{gd\ (NMOS,\ OFF)} + 2C_{gs\ (NMOS,\ ON)} + 4C_{gd\ (NMOS,ON)}$$

$$C_{out} = 2C_{dg(NMOS,ON)} + 2C_{dg(PMOS,\ OFF)}$$
$$= 2C_{dg(NMOS,ON)} + 4C_{dg(NMOS,\ OFF)}$$

$$C_{eff} = C_{in} + C_{out} + C_L$$

Fig 8 shows the obtained delay vs. T_{spacer} for C_L=0 and C_L=*0.1pF*.

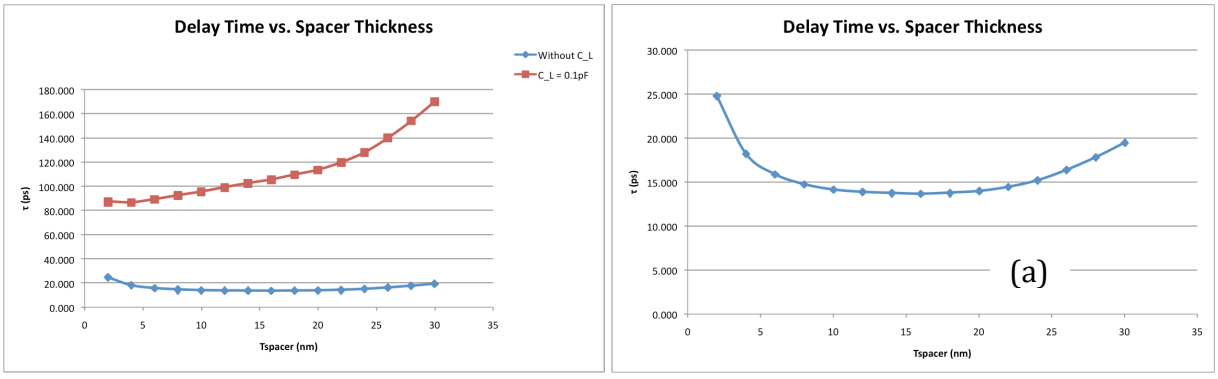

Fig 8: delay vs. T_{spacer} for (a): C_L=*0* (b): C_L= *0.1pF*

A) Optimal T_{si} :

The delay is a tradeoff between parasitic capacitance and parasitic resistance or equivalently a tradeoff between C_{eff} and I_{eff}. At lower T_{spacer} the S/D doping overlaps and the parasitic overlap capacitances are large; at higher T_{spacer} this overlap is decreased, C_{eff} is reduced, and the time delay time is increased.

for much higher Tsp the channel resistance becomes large or Ieff reduces and the delay increases again. The optimal value of Tsp is at **16nm** and its associated delay is **13.6ps**.

When C_L = 0.1pF, the minimum delay time constant cannot be found as easily as the case with C_L=0. Nonetheless, we approximate the optimal T_{spacer} to be around 5nm. Thus, adding an external load to the system decreases the optimal spacer thickness. The reason for this observation is that while Ceff is changed by C_L, Ieff is roughly unchanged and as result the tradeoff between Ieff and Ceff leads to a lower optimal T_{spacer} as compared to the case of CL=0. In addition, in Fig. 8, the delay plot for CL=0.1pF is shifted up to higher delay ranges because the C_{eff} is increased by a factor of C_L (R_{eff} is roughly constant here).

A) Effect of Doping Gradient:

In Fig 10, the effect of using abrupt doping profile in S/D is simulated. If S/D doping characteristic length is more abrupt, S/D gate overlap reduces and induces more parasitic resistance. Therefore, we see an increase in delay for higher T_{sp}. Also, the C_{in} (Fig 9) can be increased more when there is abrupt doping in S/D but the effect of increasing extrinsic resistance for higher T_{sp} is more serious than the effect of inducing C_{in} at lower T_{sp}.

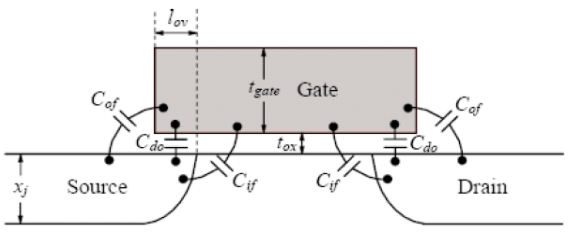

Fig 9: fringing and overlap gate capacitance

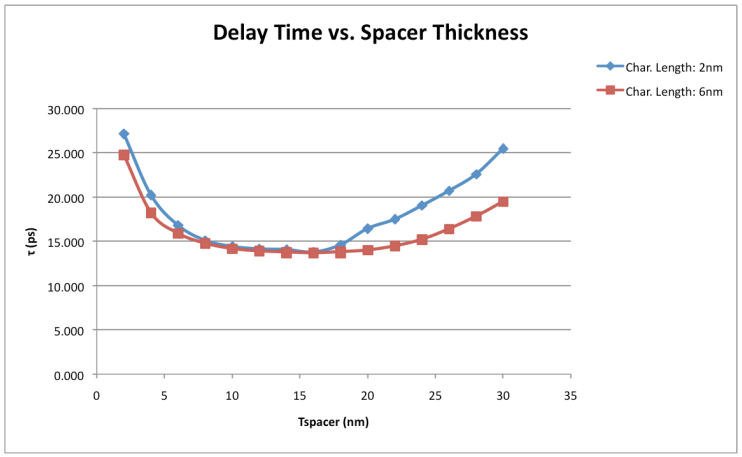

Fig 10: Delay vs. Spacer Thickness for 2 cases of doping characteristic length 6 and 2nm.

B) Effect of Spacer Dielectric Constant:

By decreasing the dielectric constant, we expect to have a larger delay as the gate capacitances start increasing. This effect is very well illustrated for small T_{spacer} values in Fig. 11. In other words, the value of C_{gd} and C_{gs} are proportional to $\varepsilon_{dielectric}/T_{sp}$. Thus, C_{eff} decrease by lowering the dielectric constant. However, for larger T_{spacer} values, the two delays are roughly the same as another effect starts dominating the delay performance: large T_{spacer} values prevent fringing effects and consequently decrease the fringing capacitance between S/D electrodes and the gate.

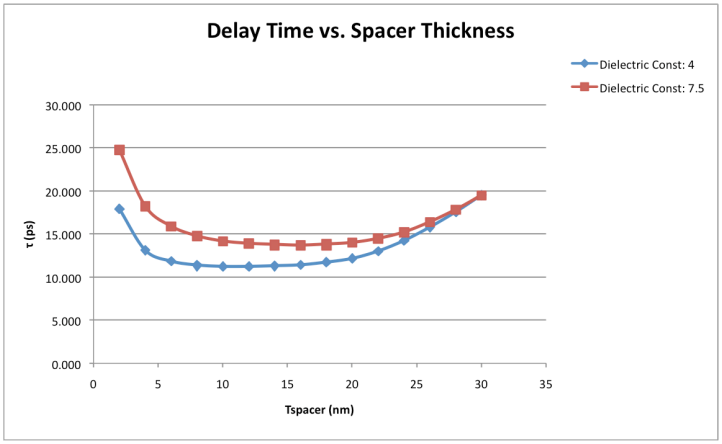

Fig.11: delay vs. spacer thickness for 2 dielectric constants 7.5 and 4.

C) Effect of H_{raise}:

The raised source and drain are designed to reduce the series resistance for the case of a finite contact resistance between the contact metal and the semiconductor. In this project, the contact resistance is assumed to be zero for simplicity; therefore, the value of H_{raise} for the raised source/drain has little effect on resistance or on changing I_{eff}. In fact, from Fig 12a, it turns out that the above assumption is fairly reasonable as the effective current of the device stays unchanged when H_{raise} varies.

Increasing H_{raise}, increases the fringing parasitic capacitance and hence the effective capacitance (see Fig 12b). Thus, because C_{eff} increases while I_{eff} stays roughly fixed (see Fig 12), the overall RC delay is expected to increase as illustrated in Fig 13.

Additionally, as shown in the table below, the optimal T_{spacer} shifts to higher values due to

1) very large capacitance differences in small T_{spacer} values and negligible differences in large T_{spacer} values.
2) decrease in R with increasing H_{raise}. Recall that delay is a tradeoff between capacitance and resistance.

H_rise (nm)	Optimal Tsp (nm)
10	10
40	16
55	16

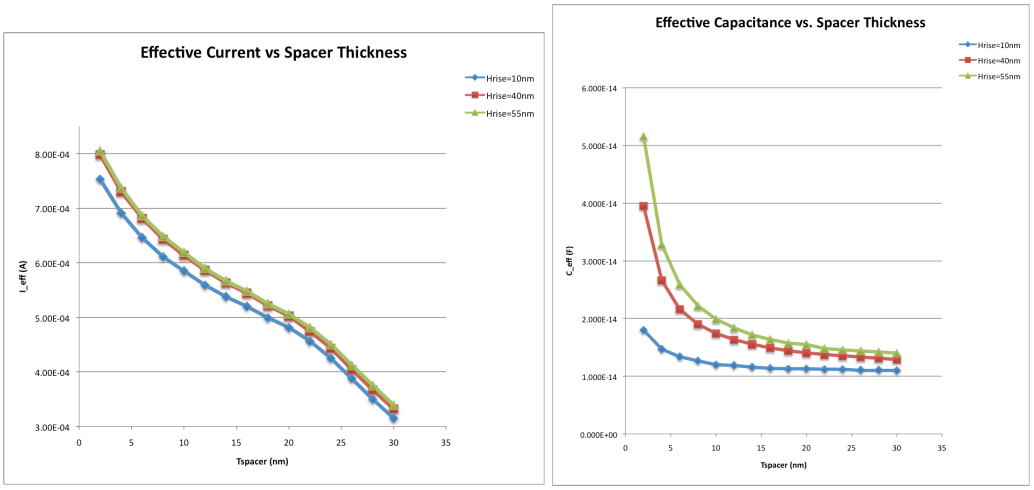

Fig. 12: (a) I_{eff} and (b) C_{eff} vs. T_{sp} for H_{raise}= *10nm, 40nm* and *55nm*.

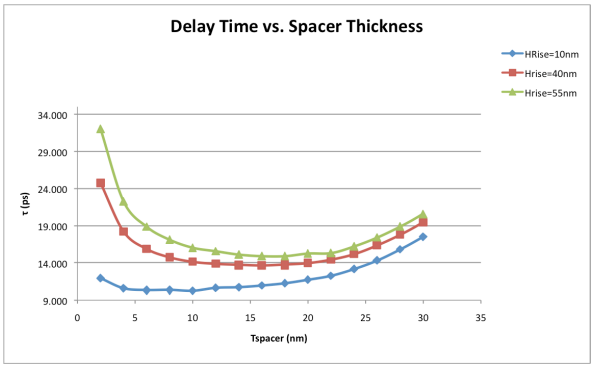

Fig. 13: delay vs. T_{sp} for H_{raise}=*10nm, 40nm* and *55nm.*

CONCLUSION

We have seen that parasitic capacitance and extrinsic resistance limits performance in ultrathin body DGFETs. In order to minimize the impacts of these parasitic elements, it is desired to engineer the structure such that the device performance and power consumption are optimized. The raised source/drain structure allows increasing the effective contact area and the effective on-current. With choosing specific lateral characteristic length for the S/D doping, the optimum value of spacer thickness is obtained at which the delay is minimized. This optimization involves balancing the impact of short channel effects and series resistance.

References:

[1] R.S. Shenoy and K.C. Saraswat, “Optimization of Extrinsic Source/Drain Resistance in Ultrathin Body Double-Gate FETs”, IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 2, NO. 4, 2003.

[2] D.J. Frank, “Device Scaling Limits of Si MOSFETs and Their Application Dependencies”, PROCEEDINGS OF THE IEEE, VOL. 89, NO. 3, 2001

[3] M. Na et al., “The effective drive current in CMOS inverters,” IEDM, pp.121-124, 2002.

Appendix:

Attached are .scm file and .cmd files.