TP 14.2 A CMOS Analog Front-End IC for DMT ADSL

Cormac Conroy, Samuel Sheng, Arnold Feldman[1], Gregory Uehara[2], Alfred Yeung, Chih-Jen Hung, Vivek Subramanian, Patrick Chiang[3], Paul Lai, Xiaomin Si, Jerry Fan, Denis Flynn, Meiqing He

DataPath Systems, Inc., Los Gatos, CA
[1]Now at Level One Communications, San Francisco, CA
[2]University of Hawaii at Manoa, Honolulu, HI
[3]Now at Stanford University, Stanford, CA

Asymmetric digital subscriber line (ADSL) technology meets the need for high-bandwidth communications to the home utilizing the existing twisted-pair copper. In an ADSL modem, noise and linearity of the analog front end (AFE) are critical to the data rate achievable over the longest lines (up to and above 18kfeet of AWG24 wire) and hence the fraction of installed lines over which ADSL service can be deployed. Previously-published ADSL AFEs consist of either (a) CMOS solutions with linearity of the entire receive (RX) and transmit (TX) signal paths in the 10b to 11b range and with input-referred noise at -140dBm/Hz to -150dBm/Hz level (relative to 100Ω) [1-4]; or (b) higher-power±5V multichip BiCMOS solutions [5]. Moreover, traditional static linearity parameters such as INL and DNL, while important, are insufficient to characterize AFE performance. In multitone ADSL, dynamic linearity throughout the band determines modem capacity. This highly-integrated CMOS AFE is compatible with both the full ADSL T1E1.413 DMT standard and the emerging G.lite standard, andachieves 14b linearity in both RX and TX paths and input-referred noise better than -160dBm/Hz, from a single 5.0V supply. These noise and linearity specifications are necessary for an ADSL modem to operate at 1.5Mb/s on the longest lines and reach >90% of installed copper connections.

A block diagram is shown in Figure 14.2.1. In the RX path, the incoming analog signal has 8Vppd peak level. Two programmable gain amplifier (PGA) stages provide aggregate gain from -6dB to +38dB with better than 0.25dB resolution. The 4th-order lowpass RX filter is a cascade of two 2nd-order Butterworth lowpass sections and uses a continuous-time active R-C topology. Two versions of the chip exist: one for the customer remote modem (ATU-R) and one for the central office (ATU-C). In the ATU-R, the aggregate filter cutoff frequency (f_c) is programmable to either 1.104MHz or 552kHz (for G.lite); in the ATU-C, f_c is programmable to either 138kHz or 276kHz (for operation of ADSL over ISDN). The filter output is digitized by a 16b-resolution ADC at either 4.416M or 2.208MSample/s. The ADC uses a switched-capacitor digitally-calibrated multistage pipeline with high-gain OTA to minimize calibration drift over temperature (Figure 14.2.2).

Input-referred noise power spectral density (PSD) of the entire ATU-R RX path including ADC is given in Figure 14.2.3 along with the PGA+filter frequency response. The measured PSD of -162dBm/Hz (2.5nV/√Hz) at frequencies around 300kHz ensures that the AFE noise contribution is negligible compared to the nominal line noise of -140dBm/Hz and enables modem payload to be maximized over the longest lines where SNR is critical. Low-frequency linearity of the RX section (PGA+filter+ADC) is shown in Figure 14.2.4. The test signal is a 100kHz/110kHz 2-tone pattern generated by the DAC and TX section, and looped back through the RX section. The ADC spectrum shows the 3rd-order intermodulation distortion products below -100dBFS, ensuring that data payload can be maximized in the low bins of the ADSL band where available SNR is highest. High-frequency dynamic linearity is shown in Figure 14.2.5, which shows the ADC spectrum for a near-full-scale 900kHz sinusoid. Spurious-free dynamic range is 91dB. The inset shows ADC DNL better than ±0.5LSB at a 16b level from a low-frequency histogram test.

The TX section consists of two identical signal paths: one for the primary TX signal and one to support echo for systems using analog echo cancellation (EC). A single DAC is shared between the two paths minimizing difficulties in analog EC arising from distortion mismatch between two DACs. The 16b-resolution DAC uses a switched-capacitor digitally-calibrated multistage architecture. The DAC output voltage is re-sampled to remove code-dependent glitches that would degrade dynamic linearity. In frequency division multiplexing (FDM) systems, the echo path is not used, and incoming digital data is fed to the DAC at 4.416MHz. In EC systems, data is fed at 8.832MHz and alternate DAC outputs are transferred in ping-pong fashion to the primary TX and echo path filters. Each filter is a 4th-order lowpass, comprising two 2nd-order Butterworth sections; f_c is 1.104MHz for ATU-C, and 138kHz or 276kHz for ATU-R, depending on ISDN mode. To simplify overall system design, DAC droop compensation is incorporated in the filter. The TX programmable attenuator range is 0 to -18dB with better than 1dB resolution. The differential outputs can drive an ac-coupled 2kΩ load with 5Vppd maximum signal level.

Overall AFE linearity is tested by feeding a DMT-like multitone waveform through the DAC/TX section and looping back through the RX/ADC section. The test signal consists of 248 tones over the 1.104MHz band with 8 missing tones or "holes" in the spectrum. Intermodulation distortion products from tones throughout the spectrum will fall into the "holes", thereby degrading SNDR in these frequency bins, and hence limiting modem data rate capacity. The relative phases of the tones are chosen so the waveform peak-to-average-ratio (PAR) is 7.7dB, which is more demanding from a linearity standpoint than a true DMT signal with 15dB PAR. The ADC spectrum shows multitone power ratio (MTPR) better than 81dB at the holes at 349kHz, 487kHz, and 625kHz, spanning the center of the ADSL downstream band (Figure 14.2.6).

The ADC and DAC full scale ranges (5Vppd) are set by internal reference voltages. Digitally-calibrated bandgap references minimize absolute spread over process corners. Better than ±5% absolute accuracy on filter f_cs is achieved using an on-chip tuning algorithm. The IC requires no external circuitry beyond two precision resistors and bypass/coupling capacitors, and requires no factory trimming. All calibration isd one at reset by an on-chip controller - no background calibration is needed. An all-analog energy detector performs the ADSL wakeup function: the wakeup signal (R-ACT-REQ in the T1E1.413 standard) is a sinusoid at either 34.5kHz or 172.5kHz (for ADSL over ISDN). The chip detects this tone, and notifies the rest of the modem by asserting a digital output. Most of the ATU-C modem can be powered down while waiting for activity from the ATU-R, resulting in considerable power savings in the central office. A 12b monotonic voltage output DAC is also included to support an external voltage-controlled crystal oscillator. The AFE is 5.63x5.83mm² in 0.5μm double-poly triple-metal CMOS. A die micrograph is shown in Figure14.2.7. Power is 675mW in FDM mode, and 825mW in EC mode.

Acknowledgment:
The authors thank M. Agah of TI Broadband Access Group for significant contributions.

References:
[1] Shariatdoust, R., et al. "A high-speed, high-resolution analog front end for digital subscriber line applications," in Proc. CICC, May 1995, pp.13.3.1-13.3.4.
[2] Analog Devices, Inc., "AD6437, Analog Front End for ADSL".
[3] Chang, Z.-Y., et al. "A CMOS analog front-end circuit for an FDM-based ADSL system," IEEE J. Solid-State Circuits, vol. 30, no. 12, Dec. 1995, pp. 1449-1456.
[4] Alcatel Microelectronics, "MTC-20134, Integrated ADSL CMOS Analog Front-End Circuit"; and ST Microelectronics, "STLC60134, TOSCA Integrated ADSL CMOS Analog Front-End Circuit".
[5] Langford, D. S., et al., "A BiCMOS analog front-end circuit for an FDM-based ADSL system," IEEE J. Solid-State Circuits, vol. 33, no. 9, Sep. 1998, pp. 1383-1393.

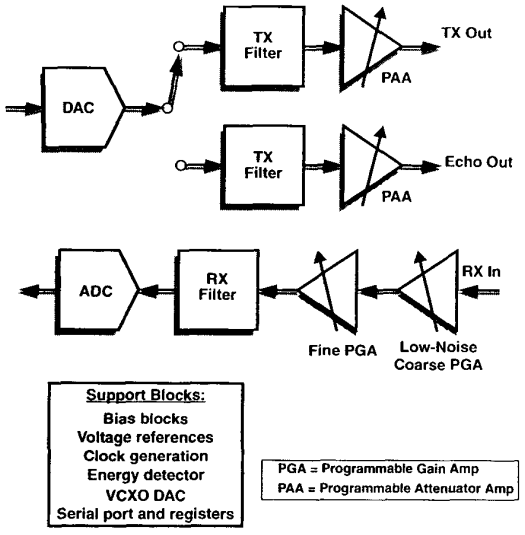

Figure 14.2.1: Chip block diagram.

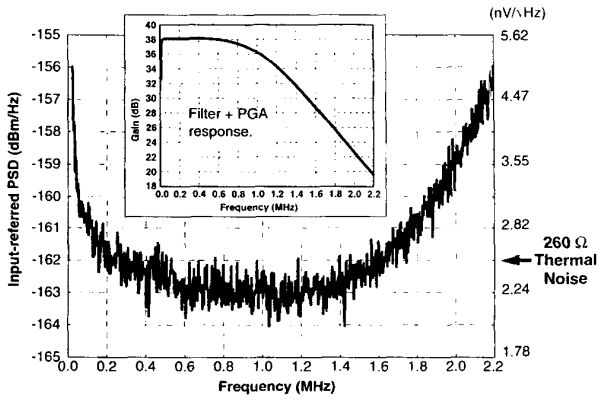

Figure 14.2.3: ATU-R noise PSD at +38dB gain. Inset: RX path transfer characteristic.

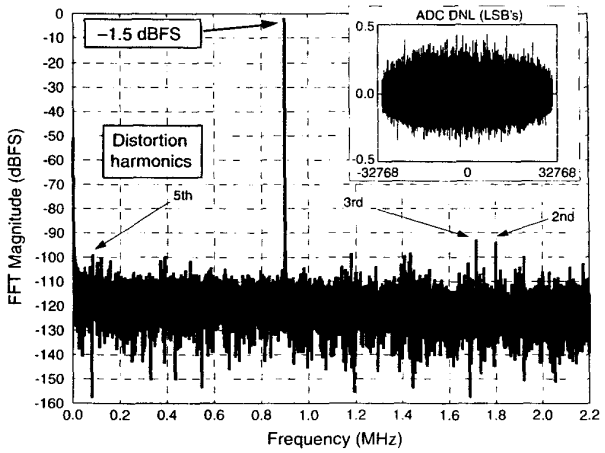

Figure 14.2.5: 32k-point FFT of ADC output showing distortion harmonics. Inset: ADC DNL at 16b level.

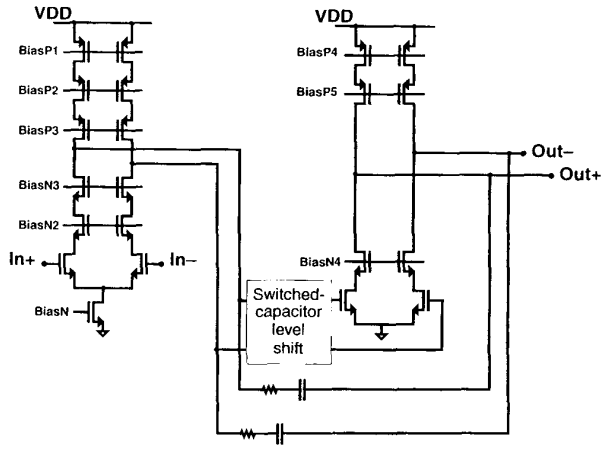

Figure 14.2.2: Simplified schematic of OTA used in ADC pipeline stage.

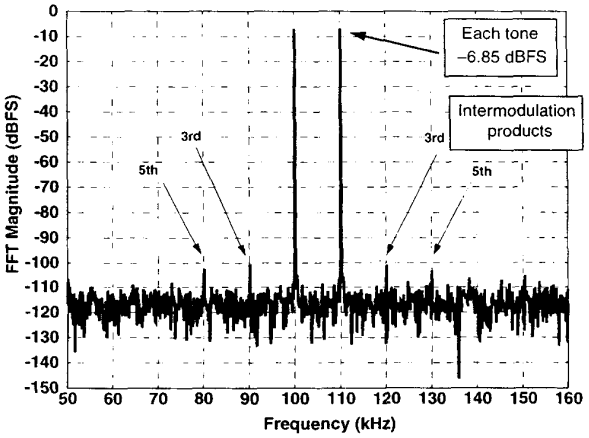

Figure 14.2.4: Zoom-in of 32k-point FFT showing odd-order intermodulation products.

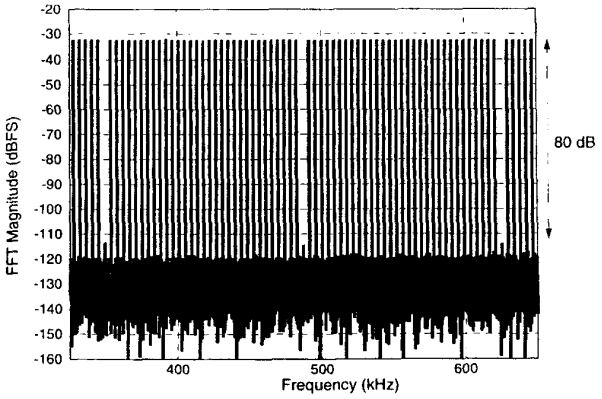

Figure 14.2.6: Portion of 256k-point FFT of combined TX and RX response for multitone signal.

Figure 14.2.7: See page 465.

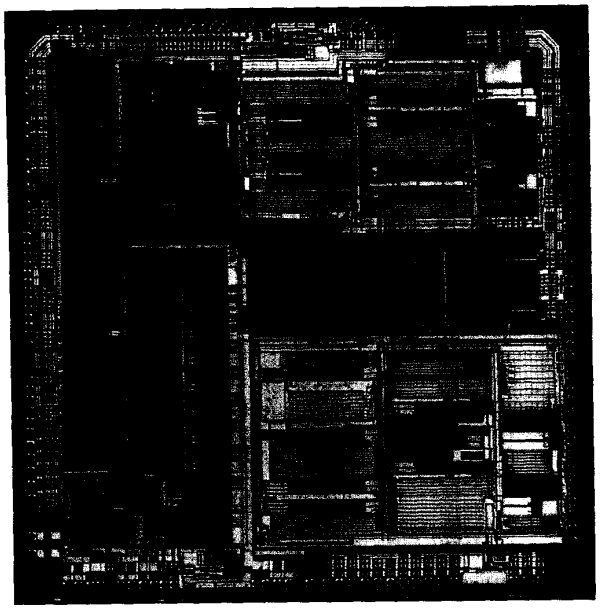

Figure 14.2.7: Die micrograph.

$$H_{LP}(\omega)=\frac{b_1Z^{-1}+b_2Z^{-1}+b_3Z^{-1}}{a_1Z^{-1}+a_2Z^{-2}+a_3Z^{-3}},$$

where $b_1=b_3=\frac{1}{128}-\frac{1}{1024}$, $b_2=-\frac{1}{128}+\frac{1}{2048}$, $a_1=2+\frac{1}{2}+\frac{1}{8}+\frac{1}{16}-\frac{1}{256}-\frac{1}{2048}$,

$a_2=-2+\frac{1}{2}-\frac{1}{16}$, $a_3=\frac{1}{2}+\frac{1}{4}-\frac{1}{512}$ and $Z=\exp\left[\frac{j\omega}{4416\,\text{kHz}}\right]$

(A)

$$H_{DEC}=\frac{1+Z^{-1}+Z^{-2}}{2+0.25Z^{-1}+Z^{-2}},\ \text{where } Z=\exp\left[\frac{j\omega}{4416\,\text{kHz}}\right]$$

(B)

Figure 14.3.4 Transfer functions of RT
(a) transmitter
(b) receiver digital filters.

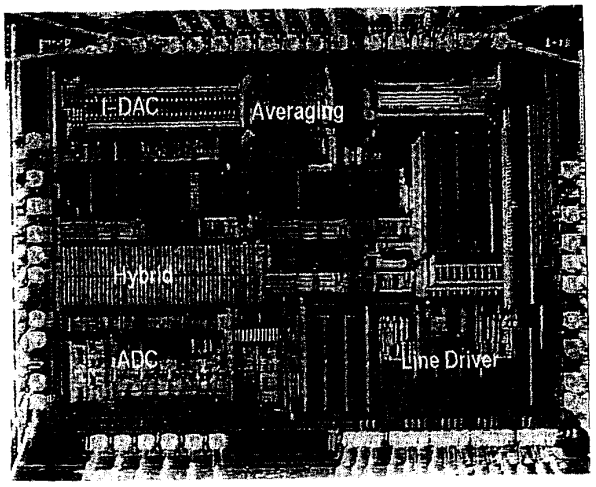

Figure 14.4.7: DSL chip micrograph.

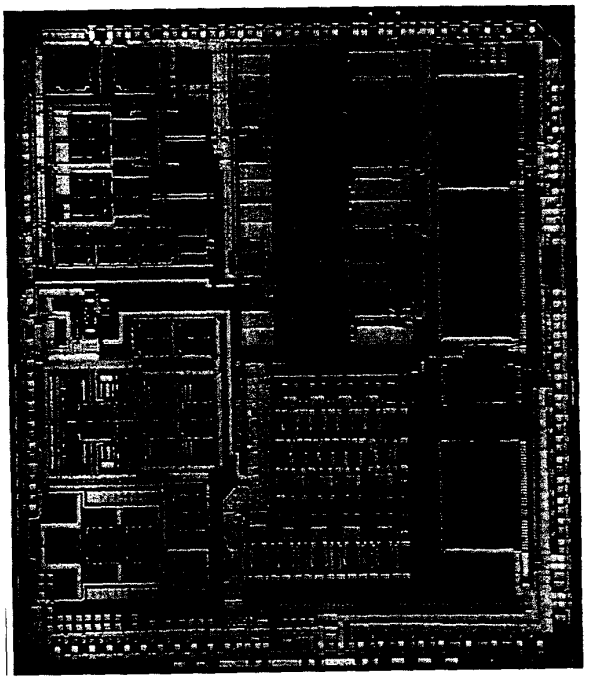

Figure 14.3.7. Chip micrograph.

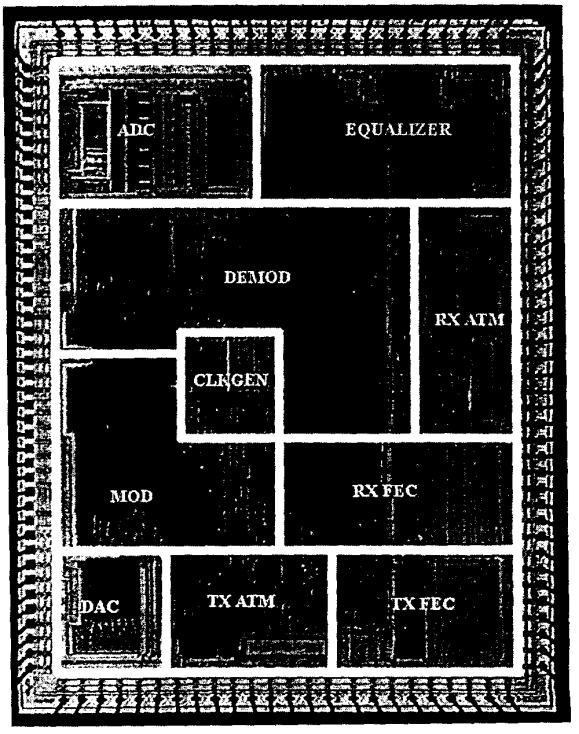

Figure 14.7.6: Universal QAM Transceiver Chip micrograph.