Patrick Yin Chiang

Gates Computer Science Building, Room 2A-212
Stanford, CA 94305
650-224-0615
pchiang@leland.stanford.edu
www.stanford.edu/~pchiang

Education

2000 - Present	***Stanford University*** Doctoral Student in Electrical Engineering Advisor: Bill Dally, Co-Advisor: Mark Horowitz Thesis: Precision Clock Synthesis Using Direct Modulation of Front-End Multiplexers/Demultiplexers in High Speed Serial Links	Stanford, CA
1998 - 2001	***Stanford University*** M.S. Electrical Engineering	Stanford, CA
1993 - 1997	***University of California, Berkeley*** B.S. Electrical Engineering and Computer Sciences (Magna Cum Laude) Honor Societies: Eta Kappa Nu, Tau Beta Pi	Berkeley, CA

Experience

1998 - present	***Stanford University*** – Research Assistant ▪ Design/implementation/fabrication of 2nd generation 20Gb/s 0.13um CMOS transceiver, including receiver demultiplexer, on-die BER measurement, transmitter 2-Tap equalization. Designed CAD flow for analog design/extraction/simulation, fabricated testboards, and helped coordinate liaison with industrial foundry ST Microelectronics. ▪ Designed and fabricated a 20Gb/s 0.13um CMOS serial link transmitter, using direct modulation of the transmitter multiplexer with the LC Oscillator. Exhibits lower area/power/complexity and higher data rate than current conventional architectures. Includes 10GHz LC-Phase Locked Loop, 8:1 high speed analog transmitter multiplexing, analog latch hysteresis compensation. Won design award and presented many invited presentations (Intel, Infineon, Phillips, Rambus). ▪ Assisted with design and layout of 90nm CMOS 16Gb/s Transceiver for Optical Links. ▪ Designed a 20Mb/s Ultra-Wideband Transceiver in 0.25um CMOS using chaotic pulse position modulation, representing one of the only fully integrated implementations of a non-linear communications system on a single chip. Acted on Dally's behalf as project leader of a Multi-University Research Initiative with UCSD, UCLA, and Stanford—gave Department of Defense technical reviews, talks, and proposal summaries. Project success was important in obtaining an additional year of funding for multiple university project. Contacted by many ultra-wideband chip companies (Intel, Wisair, Aether-Wire) for possible commercialization. ▪ Worked on a low power 0.25um 4Gb/s serial link transceiver, burning 140mW/link and 20mV input sensitivity. Research became key intellectual property for Velio (now Rambus). ▪ Designed and fabricated an electrically addressable, liquid release well array for a handheld dispense system, sponsored by Mechanical Engineering Department and Agilent Technologies.	Stanford, CA
Fall 2004	***Telegent Systems –*** Consultant ▪ Compared and simulated wideband VCO/PLL architectures for direct conversion CMOS tuner.	Sunnyvale, CA
2003	***Velio Communications (now Rambus)*** – Research Intern ▪ Evaluated various 10GHz clocking synthesizers for next generation serial link cores.	Milpitas, CA
1997 - 1998	***Datapath Systems (now LSI Logic)*** – Design Engineer ▪ Created and designed a 100 cell automated standard cell library for a 0.5um process. ▪ Designed backend digital logic for 14bit, 8MHz pipelined A/D converter. ▪ Designed switch-capacitor integrator with chopper stabilization for low power mode.	Los Gatos, CA
1996 - 1997	***Electronics Research Laboratory (UC Berkeley)*** – Senior Engineering Aide ▪ Designed 200 VHDL cell descriptions for low power standard cell library. ▪ Designed, synthesized, and simulated a burst read-write controller for a low power SRAM.	Berkeley, CA

Teaching

Win 2001	***Stanford University*** – Teaching Assistant ▪ Conducted review sessions, led discussions for course of 90 graduate students for high speed signal integrity course. ▪ Graded exams, class project of a high speed signaling bus architecture.	Stanford, CA
Win 2000	***Stanford University*** – Teaching Assistant ▪ Conducted review sessions, led discussions for course of 110 students for high speed signal integrity course. ▪ Graded exams, graded class project of backplane router signaling system.	Stanford, CA
Fall 1996	***University of California at Berkeley*** – Teaching Assistant ▪ Conducted discussions, supervised/graded projects for digital logic design course.	Berkeley, CA

Publications

Dec 2005	T. Lamers, P. Chiang, R. Flynn, Y.R. Rau, K. Ioakeimidi, S. Devasenathipathy, B. Chui, B.L. Pruitt. An Electrically Addressable, Liquid Release Well Array for a Hand-held Scented Material Dispense System. In Submission to Hilton Head MEMS Conference 2006.	Hilton Head, SC
Dec 2005	Patrick Chiang, William J. Dally, Ming-Ju Edward Lee. A 20Mb/s Ultra-Wideband Transceiver in 0.25um CMOS Using Chaotic Pulse Position Modulation. In preparation.	Stanford, CA
Apr 2005	Patrick Chiang, William J. Dally, Ming-Ju Edward Lee, Ramesh Senthinathan, Yangjin Oh, and Mark Horowitz. "A 20Gb/s 0.13um CMOS Serial Link Transmitter Using an LC-PLL to Directly Drive the Output Multiplexer." IEEE Journal of Solid-State Circuits, Apr. 2005, Vol. 40, No. 4, pp. 1004-1011.	Stanford, CA
June 2004	Patrick Chiang, William J. Dally, Ming-Ju Edward Lee, Ramesh Senthinathan, Yangjin Oh, and Mark Horowitz. "A 20Gb/s 0.13um CMOS Serial Link Transmitter Using an LC-PLL to Directly Drive the Output Multiplexer." VLSI Circuits Symposium, Honolulu, Hawaii, June 2004.	Honolulu, HI
Aug 2002	Patrick Chiang, William J. Dally, Ming-Ju E. Lee. "A 20Gb/s 0.13um CMOS Serial Link." Hotchips 2002, Stanford, CA, Aug. 18-20,2002	Stanford, CA
June 2001	Ming-Ju E. Lee, William J. Dally, John W. Poulton, Patrick Chiang, Stephen F. Greenwood. "An 84-mW 4Gb/s Clock and Data Recovery Circuit for Serial Link Applications." VLSI Circuits Symposium, Kyoto, Japan, June 2001, pp. 149-152.	Kyoto, Japan
May 2001	Patrick Chiang, William J. Dally, Ming-Ju E. Lee. "Monolithic Chaotic Communications System." 2001 IEEE International Conference on Circuits and Systems, Sydney, Australia, May 6-9, 2001.	Sydney, Australia
Nov. 2000	Ming-Ju E. Lee, William Dally, Patrick Chiang. "Low-Power Area-Efficient High-Speed I/O Circuit Techniques." IEEE Journal of Solid-State Circuits, Nov. 2000, Vol. 35, No. 11, pp. 1591-1599.	San Francisco, CA
Feb. 2000	Ming-Ju E. Lee, William Dally, Patrick Chiang. "A 90mW 4Gb/s Equalized I/O Circuit with Input Offset Cancellation." International Solid State Circuits Conference, San Francisco, February 2000, TP 15.3, pp. 252-253.	San Francisco, CA
Feb. 1999	Cormac Conroy, Samuel Sheng, Arnold Feldman, Greg Uehara, Albert Yeung, Chih-Jen Hung, Vivek Subramanian, Patrick Chiang, Paul Lai, Xiaomin Si, Jerry Fan, David Flynn, Meiqing He. "A CMOS Analog Front-End IC for DMT ADSL." International Solid State Circuits Conference, San Francisco, February 1999, pp. 240-241.	San Francisco, CA

Invention Disclosures

Aug 2005	T. Lamers, P. Chiang, R. Flynn, Y.R. Rau, S. Devasenathipathy B.L. Pruitt. "An Electrically Addressable, Liquid Release Well Array for a Hand-held Scented Material Dispense System." Invention disclosure 22367. Stanford University Office of Technology and Licensing.	Stanford, CA
June 2004	Frank O'Mahony and Patrick Chiang. "Micromachined Slow Wave Resonator with Capacitive Cross Ties." Provisional Patent Application S04-109/PROV. Stanford University Office of Technology and Licensing.	Stanford, CA
Jan 2004	Patrick Chiang and William J. Dally. "Transceiver Clock Timing Generation by Direct Modulation from Phase/Delay Locked Loop." S04-092. Stanford University Office of Technology and Licensing.	Stanford, CA

Selected Invited Talks/Conference Presentations

June 2004	"A 20Gb/s 0.13um CMOS Serial Link Transmitter Using an LC-PLL to Directly Drive the Output Multiplexer." VLSI Symposium on Circuits.	Honolulu, HI
June 2004	"A 20Gb/s 0.13um CMOS Serial Link Transmitter Using an LC-PLL to Directly Drive the Output Multiplexer." Luxtera Corporation.	San Diego, CA
Mar 2004	"A 20Gb/s 0.13um CMOS Serial Link Transceiver." Intel Corporation.	Santa Clara, CA
June 2002	"A 20Gb/s 0.13um CMOS Serial Link Transceiver." Philips Semiconductor.	Eindhoven, Netherlands
June 2002	"A 20Gb/s 0.13um CMOS Serial Link Transceiver." Infineon Technologies.	Munich, Germany
June 2001	"An 84mW 4Gb/s Clock and Data Recovery Circuit for Serial Link Applications." VLSI Symposium on Circuits.	Kyoto, Japan
June 2001	"A Monolithic Chaotic Communications System." Department of Defense Multi-University Research Initiative Final Review.	Arlington, VA
May 2001	"A Monolithic Chaotic Communications System." International Symposium on Circuits and Systems.	Sydney, Australia

Supplementary Information

Apr 2005	BASES (Business Association of Stanford Engineering Students) Innovator's Challenge Award for thesis work.(Berkeley, Stanford, Caltech engineering competition)	Stanford, CA
July 2003	Started reading/brainstorming/paper review group on applications of silicon for biological detection.	Stanford, CA

References

Professor William J. Dally Chairman, Computer Science Stanford University Gates Computer Science, Room 301 353 Serra Mall, Stanford, CA 94305 billd@csl.stanford.edu	Professor Mark Horowitz Director, Computer Systems Laboratory Stanford University Gates Computer Science, Room 306 353 Serra Mall, Stanford, CA 94305 horowitz@ee.stanford.edu	Professor Lawrence Larson Director, Center for Wireless Communications University of California, San Diego Room 3808, EBU-I, La Jolla, CA 92093 larson@ece.ucsd.edu
Assistant Professor Beth Pruitt Mechanical Engineering, Stanford Durand Building, Room 281 496 Lomita Mall, Stanford, CA 94305 pruitt@stanford.edu	Dr. Samuel Sheng CTO, Telegent System 555 N. Mathilda Ave., #110 Sunnyvale, CA 94085 ssheng@telegentsystems.com	