

The Solution: Efficient Embedded Computing

A scalable, hierarchically-tiled programmable architecture targeted at embedded image and signal processing.

Quantify inefficiencies in processors:

- Instruction Supply & Storage
- Data Supply & Storage
- Computation

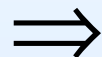
Address inefficiencies at all levels:

- Circuits
- Architecture
- Programming System

Computation

•Execution

- Pipeline registers
- Dynamic instruction scheduling

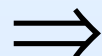


•Execution

- Exposed pipeline
- Static, power-aware scheduling

•Instructions

- Generic instructions
- Index calculations

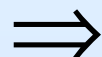


•Instructions

- Compound Instructions
- Address generators for data and register files

•Data Path

- Full-swing for speed

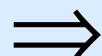


•Data Path

- Low-swing for energy

•Performance

- Ad-hoc TLP
- SIMD
- Dynamic ILP



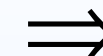
•Performance

- Power-aware partitioning
- Multi-level SIMD
- Static ILP via VLIW & MIMD

Instruction Supply & Storage

•Instruction Cache

- Large RAM to capture working set
- Tag storage and comparison
- Fixed-width instructions

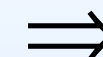


•Instruction Register Files

- Small, distributed RAMs
- Statically scheduled
- Factored instructions

•Loops

- General purpose registers used for loop counters



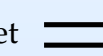
•Loops

- Dedicated iteration counters (ZOL)
- Indexable register files
- Memory DMA

Data Supply & Storage

•Data Cache

- Large RAM to capture dynamic working set
- Tag storage and comparison
- Hardware coherency

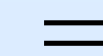


•Local Memories

- Small, distributed RAMs
- Software-controlled
- No hardware coherency

•Register Files

- Large
- Centralized, multi-ported register files



•Register Files

- Small
- Distributed
- Hierarchical
- Indexable
- Low-swing