VLSI Datapath Choices:
Cell-Based Versus Full-Custom

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Design Options

- **FPGA**
- **Standard-Cell**
- **Full-Custom**

**INCREASING**
- Quality
- Customization
- Effort
### Example: 0.25μm Technology

<table>
<thead>
<tr>
<th></th>
<th>FPGA</th>
<th>Standard-Cell</th>
<th>Full-Custom</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Xilinx XC4000CV</strong></td>
<td>25M T's</td>
<td>13.6M T's (est)</td>
<td>15.2M T's</td>
</tr>
<tr>
<td></td>
<td>100MHz</td>
<td>400MHz (est)</td>
<td>700MHz</td>
</tr>
<tr>
<td></td>
<td>&lt; 500K Gates</td>
<td>&lt; 3400K Gates</td>
<td>Not Applicable</td>
</tr>
<tr>
<td><strong>IBM SA-12</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Alpha KP21264</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Not Applicable
Full-Custom Quality with Standard Cell Effort

- Limits of Cell-Based Datapath
- Crafted-Cell Method
- Application Examples:
  - Microprocessor Register Fetch Stage
  - 64-bit Adder
  - Full-Custom vs Crafted-Cell
  - vs Standard Cell
Datapaths

- Structurally Regular
- Composed of Bit-slices
- Apply operation to $n$-bits
- Examples: Register Files, Adders, Multipliers
MIT MAP Chip Design

- 64b Multi-ALU Processor
- 6 IU’s, 1 FPU, 32KB Cache
- 5M T’s - 2.7M Memory
  2.3M Logic
- Mix of Full-Custom and Cell-based components
- Complexity Similar to HP PA8000 & Sun Ultra I
Limits: Grids

POTENTIAL PENALTY: 16% - 21%

- Lose 1 X-track & 1 Y-track
Limits: N:P Transistor Ratio

- Datapaths Employ Smaller T's
- Datapaths are N-Dominated
<table>
<thead>
<tr>
<th>Library</th>
<th>#Cells</th>
<th>Ave T's/Cell</th>
<th>Ave Cell Area (C)</th>
<th>% N-Trans</th>
<th>N:P Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Cell</td>
<td>68</td>
<td>8.5</td>
<td>95</td>
<td>39.4</td>
<td>1:1.54</td>
</tr>
<tr>
<td>Datapath</td>
<td>66</td>
<td>9.0</td>
<td>149</td>
<td>48.9</td>
<td>1:1.04</td>
</tr>
<tr>
<td>Other Full Custom</td>
<td>50</td>
<td>13.0</td>
<td>266</td>
<td>43.9</td>
<td>1:1.33</td>
</tr>
</tbody>
</table>

**POTENTIAL PENALTY:** 27%-54%
Gate Density ($\rho_g$) &
Transistor Density ($\rho_t$)

- $\rho_g$ - cell % dedicated to "gate"
  - Area = 108 grid points
  - $\#$ T's = 2
  - $\rho_g$ = 20%

- $\rho_t$ - number of T's per routing grid point
  - Area = 60 grid points
  - $\#$ T's = 8
  - $\rho_t$ = 0.1 T's/grid
Limits: Area Utilization

- Utilization Alone
- Device Interconnect

INSUFFICIENT

IMPORTANT

0% 0.00
5% 0.02
10% 0.04
15% 0.06
20% 0.08
25% 0.10
30% 0.12

0.00 0.02 0.04 0.06 0.08 0.10 0.12 0.14
Layout Efficiency: $\eta_{\text{layout}}$

\[
\eta_{\text{layout}} = \alpha + \beta r_{\text{cell}} + \gamma_{\text{max}}
\]

\[
\alpha = 0.7 \quad \beta = 1.0
\]
Crafted-Cell Method

- Small Set of Module Specific Cells (≤10)
- Share INV’s, BUF’s, MUX’s
- Reuse Cells Whenever Possible
- Custom Placement
- Automated Routing

A *Simplification* of the Full-Custom Approach
or
An *Enhancement* to Standard Cell Methods
IRRDP Crafted-Cells

- Aligned to Routing Grid
- Explicit Pins

AREA GROWTH: 11% - 25%
## BIT-SLICE/FULL IRRDP

<table>
<thead>
<tr>
<th></th>
<th>Full-Custom</th>
<th>Crafted-Cell</th>
<th>Standard-Cell</th>
</tr>
</thead>
<tbody>
<tr>
<td>Different Cells</td>
<td>80</td>
<td>7</td>
<td>17</td>
</tr>
<tr>
<td>Size</td>
<td>1x1x</td>
<td>1.64x1.64x</td>
<td>5.25x4.5x</td>
</tr>
</tbody>
</table>

- 7 Specific vs 80 Custom Cells
- 7 Complex vs 17 Simple Cells
- Automated Placement
- LOSES Structure
- Bitslice > 97% Fill
- Full < 33% Fill
Area Growth Breakdown: +64%

- Growth in Height
  - 1.07x (15 tracks/bit vs. 14 tracks/bit)

- Growth in Width
  - +37% Within Cells
  - +2% Irregular Structures
  - +11% Additional Routing Tracks
  - +3% Well/Substrate Contacts
### Additional Experimental Results

<table>
<thead>
<tr>
<th>Design</th>
<th>Full-Custom</th>
<th>Custom Cell</th>
<th>Standard Cell</th>
</tr>
</thead>
<tbody>
<tr>
<td>IrrDP Area</td>
<td>100%</td>
<td>164%</td>
<td>1450%</td>
</tr>
<tr>
<td>Critical Path</td>
<td>100%</td>
<td>111%</td>
<td>223%</td>
</tr>
<tr>
<td>AddSub Area</td>
<td>100%</td>
<td>174%</td>
<td>120% (167%)</td>
</tr>
<tr>
<td>Critical Path</td>
<td>100%</td>
<td>117%</td>
<td>440% (270%)</td>
</tr>
</tbody>
</table>
Conclusions

- Traditional Standard Cells Make Poor Datapaths
  Too Big, Too Few, Wrong Ratio!
- Crafted-Cells Overcome Traditional Limits
  Near Full-Custom Quality w/ Standard Cell Effort!
- Crafted-Cells Successfully Applied
  IRRDP, ADDSUB, & MAP chip!
Acknowledgements - Full-Custom Baselines

- IRRDP layout - MCNC
- ADDSUB design - Parag Gupta ‘96
- ADDSUB layout - Cadence Spectrum Design