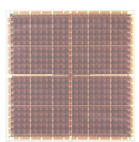
VLSI Datapath Choices:
Cell-Based Versus Full-Custom

Andrew Liang Ping Chang
Concurrent VLSI Architecture Group
Artificial Intelligence Laboratory
Massachusetts Institute of Technology
and
Computer Systems Laboratory
Stanford University

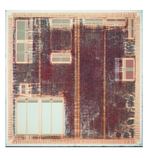
Design Options

FPGA



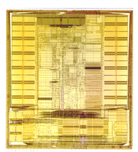
Lucent OR2C15A

Standard-Cell

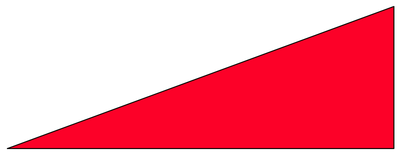


MIT Alewife A-1000 CMMU

Full-Custom



DEC ALPHA 21164



INCREASING
Quality
Customization
Effort

Example: 0.25㎜ Technology

FPGA	Standard-Cell	Full-Custom
Xilinx XC4000CV	**IBM SA-12**	**Alpha KP21264**
25M T's	13.6M T's (est)	15.2M T's
100MHz	400MHz (est)	700MHz
< 500K Gates	< 3400K Gates	*Not Applicable*

Full-Custom Quality with Standard Cell Effort

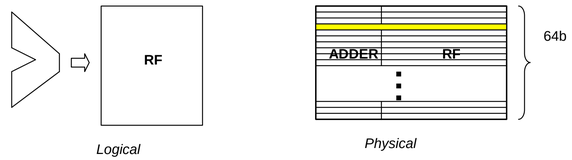
- **Limits of Cell-Based Datapath**
- **Crafted-Cell Method**
- **Application Examples:**

Microprocessor Register Fetch Stage
64-bit Adder

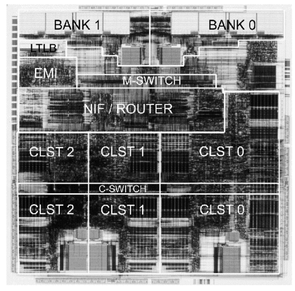
Full-Custom vs Crafted-Cell
vs Standard Cell

Datapaths

- **Structurally Regular**
- **Composed of Bit-slices**
- **Apply operation to *n*-bits**
- **Examples: Register Files, Adders, Multipliers**

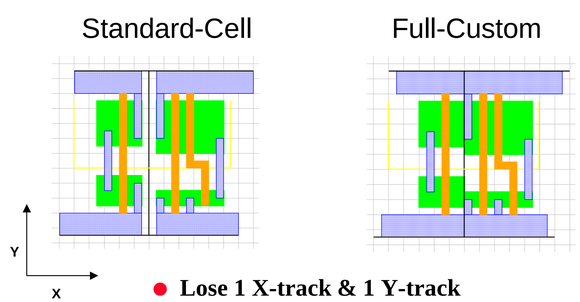


MIT MAP Chip Design



- **64b Multi-ALU Processor**
- **6 IU's, 1 FPU, 32KB Cache**
- **5M T's - 2.7M Memory**
  2.3M Logic
- **Mix of Full-Custom and Cell-based components**
- **Complexity Similar to HP PA8000 & Sun Ultra I**

Limits: Grids

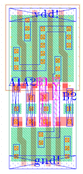


- **Lose 1 X-track & 1 Y-track**

POTENTIAL PENALTY: **16% - 21%**

Limits: N:P Transistor Ratio

Standard-Cell



AOI22

Full-Custom

MUX2

- **Datapaths Employ Smaller T's**
- **Datapaths are N-Dominated**

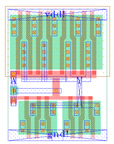
N:P Disparity

Library	#Cells	Ave T's/Cell	Ave Cell Area (C^2)	% N-Trans	N:P Ratio
Standard Cell	68	8.5	95	39.4	1:1.54
Datapath	66	9.0	149	48.9	1:1.04
Other Full Custom	50	13.0	266	43.9	1:1.33

POTENTIAL PENALTY: **27%-54%**

Gate Density (r_g) & Transistor Density(r_t)

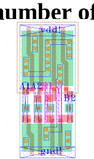
- **r_g - cell % dedicated to "gate"**



INV_16

Area = 108 grid points
#T's = 2
r_g = 20%

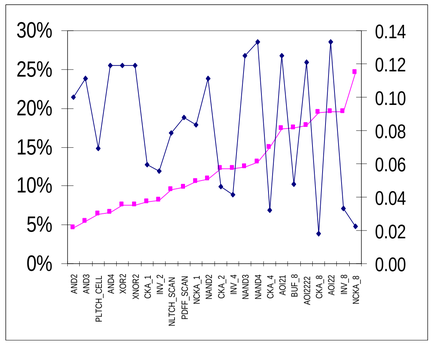
- **r_t - number of T's per routing grid point**



AOI22

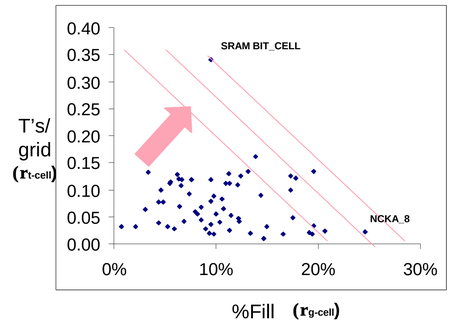
Area = 60 grid points
#T's = 8
r_t = 0.1 T's/grid

Limits: Area Utilization



- **Utilization Alone INSUFFICIENT**
- **Device Interconnect IMPORTANT**

Layout Efficiency: **h**layout



$$h_{layout} = a \frac{r_{t\text{-}cell}}{r_{t\text{-}max}} + b \frac{r_{g\text{-}cell}}{r_{g\text{-}max}}$$

a = 0.7

b = 1.0

Crafted-Cell Method

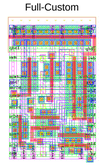
- **Small Set of Module Specific Cells (≤10)**
- **Share INV's, BUF's, MUX's**
- **Reuse Cells Whenever Possible**
- **Custom Placement**
- **Automated Routing**

A *Simplification* of the Full-Custom Approach
or
An *Enhancement* to Standard Cell Methods

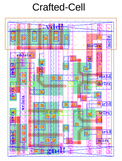
IRRDP Crafted-Cells

Register R/W

Full-Custom



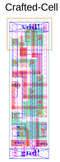
Crafted-Cell



Register Bit

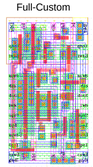
Full-Custom

Crafted-Cell

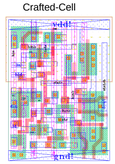


Pipeline Latch

Full-Custom



Crafted-Cell

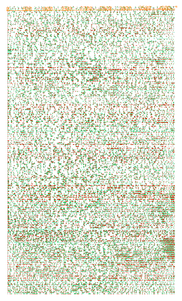


- **Aligned to Routing Grid**
- **Explicit Pins**

AREA GROWTH: 11% - 25%

BIT-SLICE/FULL IRRDP

Full-Custom	Crafted-Cell	Standard-Cell
80 Different Cells	7 Different Cells	17 Different Cells
1x/1x	**1.64x/1.64x**	**5.25x/14.5x**



- **7 Specific vs 80 Custom Cells**
- **7 Complex vs 17 Simple Cells**
- **Automated Placement LOSES Structure**
- **Bitslice > 97% Fill**
  Full < 33% Fill

Area Growth Breakdown: +64%

- Growth in Height
  - » 1.07x (15 tracks/bit vs. 14 tracks/bit)
- Growth in Width
  - » +37% Within Cells
  - » +2% Irregular Structures
  - » +11% Additional Routing Tracks
  - » +3% Well/Substrate Contacts

Additional Experimental Results

Design	Full-Custom	Crafted-Cell	Standard Cell
IRRDP *Area*	100%	164%	1450%
Critical Path	100%	111%	223%
ADDSUB *Area*	100%	174%	120% (167%)
Critical Path	100%	117%	440%(270%)

Conclusions

- Traditional Standard Cells Make Poor Datapaths
  Too Big, Too Few, Wrong Ratio!
- Crafted-Cells Overcome Traditional Limits
  Near Full-Custom Quality w/ Standard Cell Effort!
- Crafted-Cells Successfully Applied
  IRRDP, ADDSUB, & MAP chip!

Acknowledgements - Full-Custom Baselines

- **IRRDP layout - MCNC**
- **ADDSUB design - Parag Gupta ‘96**
- **ADDSUB layout - Cadence Spectrum Design**